BJT Biasing

CM

Transistor Biasing and Thermal Stabilization :

- Need for biasing
- operating point
- load line analysis
- BJT biasing- methods
- basic stability
  - Thermal runaway, Thermal stability
  - Stabilization against variations in V_{BE}, Ic, and β
  - Stability factors, (S, S', S'')
  - fixed bias
  - collector to base bias
  - self bias
  - Bias compensation,.

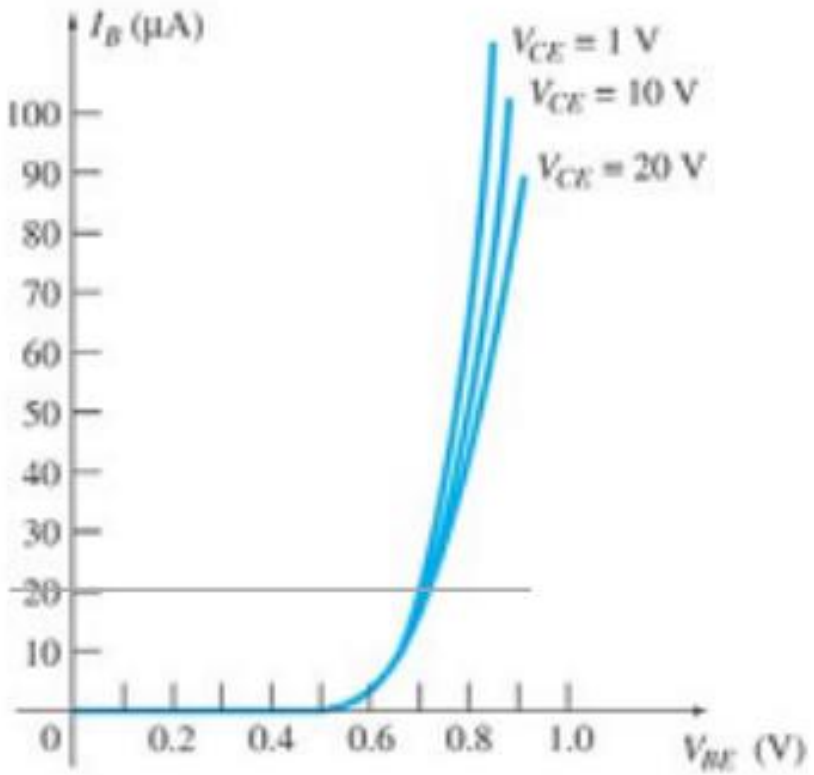
Need for BIASING?

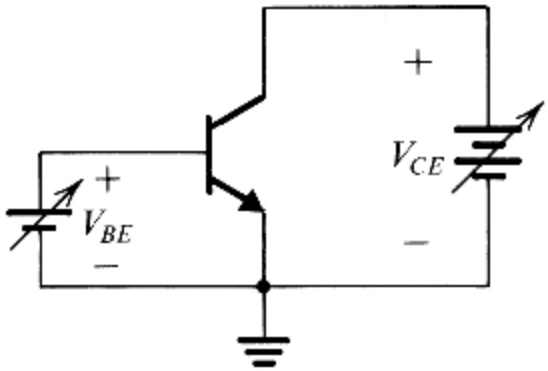
If the transistor is not biased properly, it would work inefficiently and produce distortion in output signal.

HOW CAN A TRANSISTOR BE BIASED?

A transistor is biased either with the help of battery or associating a circuit with the transistor. The later method is more efficient and is frequently used. The circuit used for transistor biasing is called the biasing circuit.

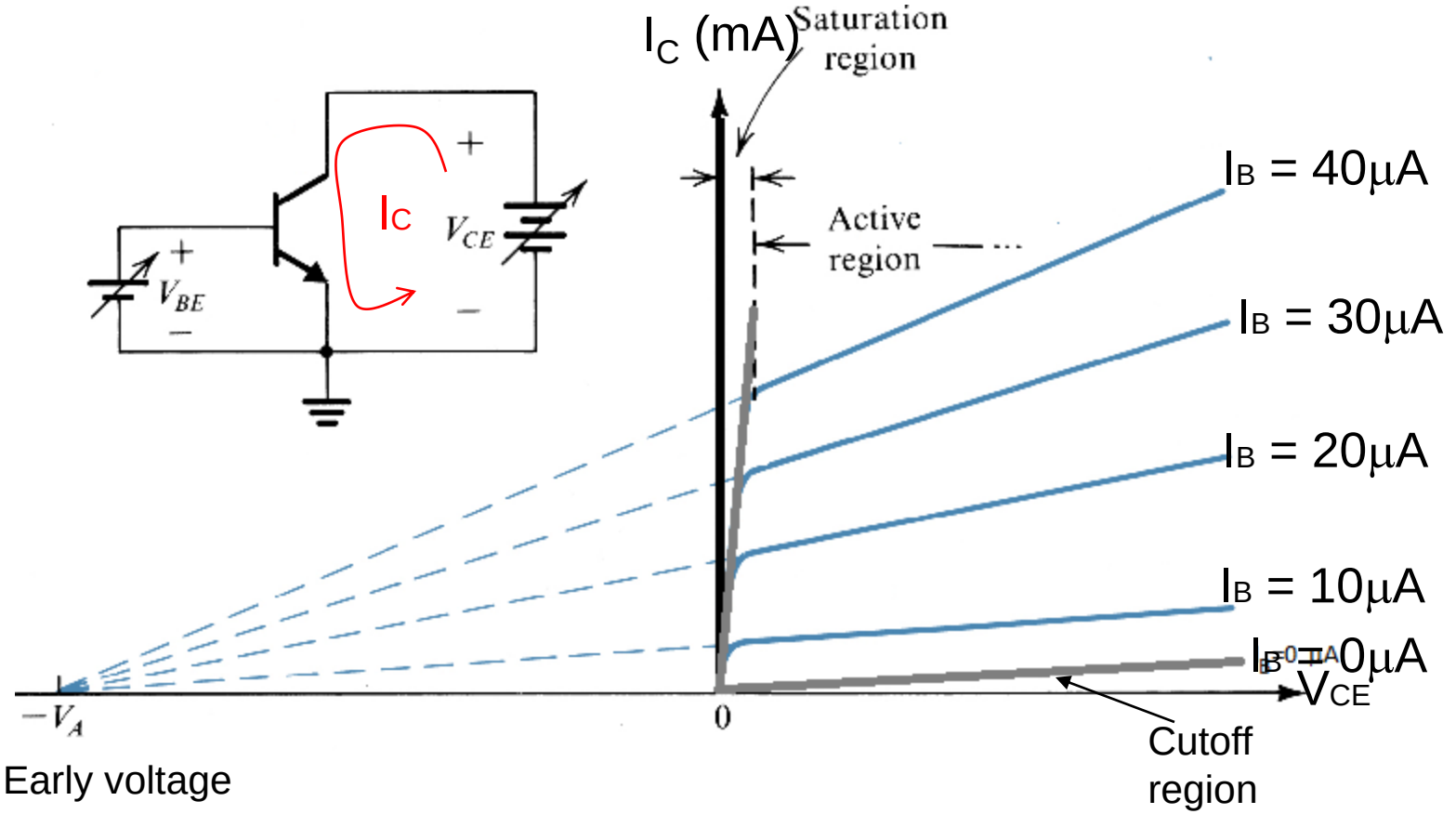
Input characteristics of npn CE mode BJT





- Acts as a diode
- $V_{BE} \approx 0.7V$

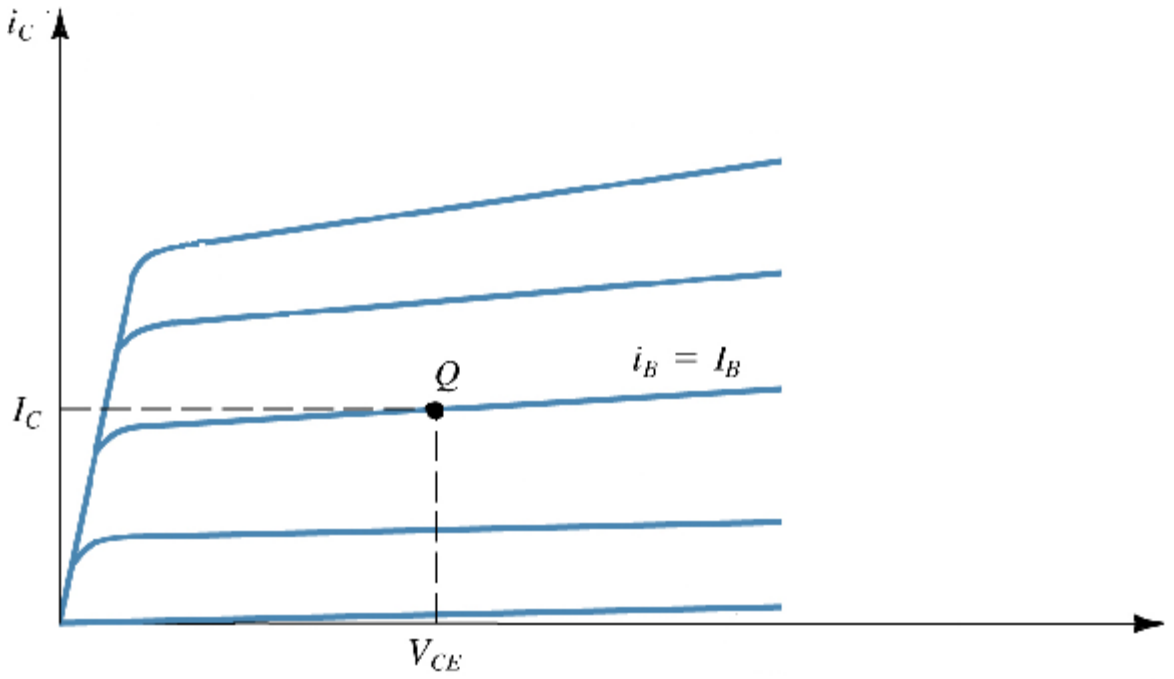
Output characteristics



- At a fixed I_B, I_C is not independent on V_{CE}
- Slope of output characteristics (output conductance) in linear region is very s

Biasing a transistor

•We must operate the transistor in the linear region.
•A transistor's operating point (Q-point) is defined by I_C, V_{CE}, and I_B.



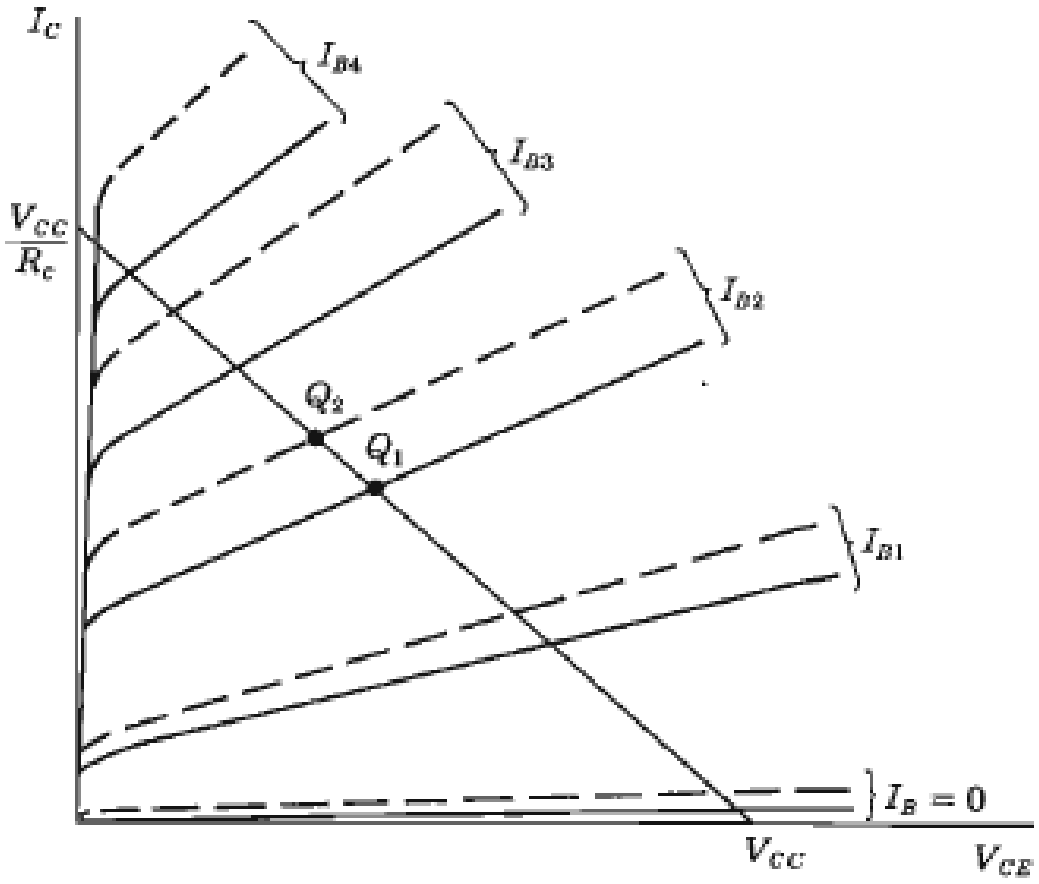
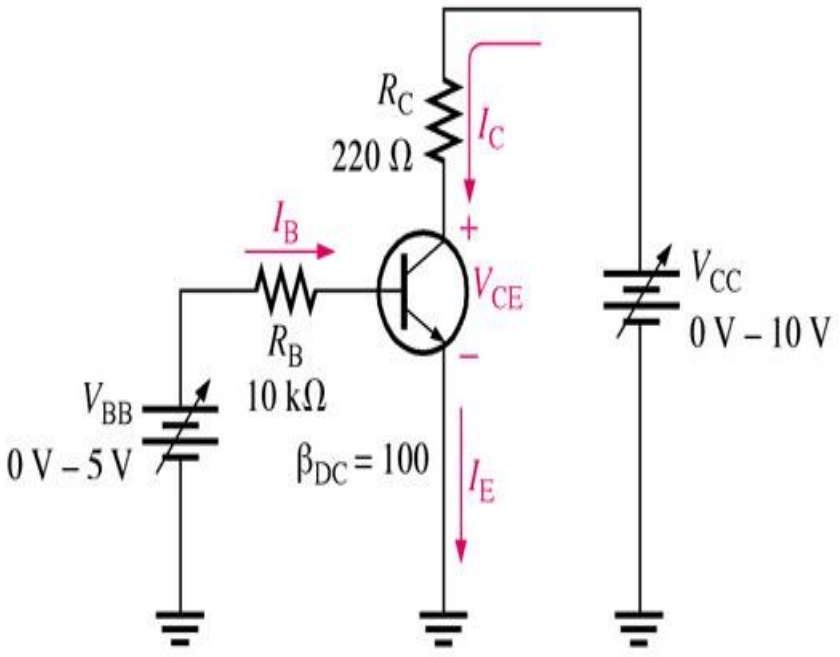


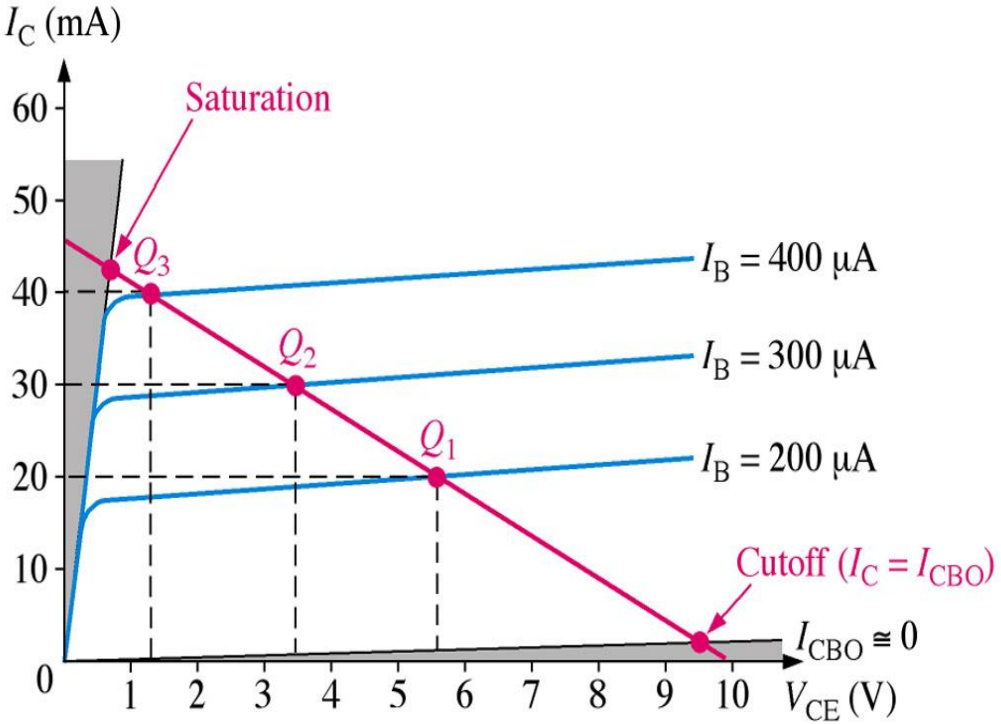
Fig. 9-3 Graphs showing the collector characteristics for two transistors of the same type. The dashed characteristics are for a transistor whose β is much larger than that of the transistor represented by the solid curves.

The DC Operating Point

For a transistor circuit to amplify it must be properly biased with dc voltages. The dc operating point between saturation and cutoff is called the **Q-point.** The goal is to set the Q-point such that that it does not go into saturation or cutoff when an a ac signal is applied.

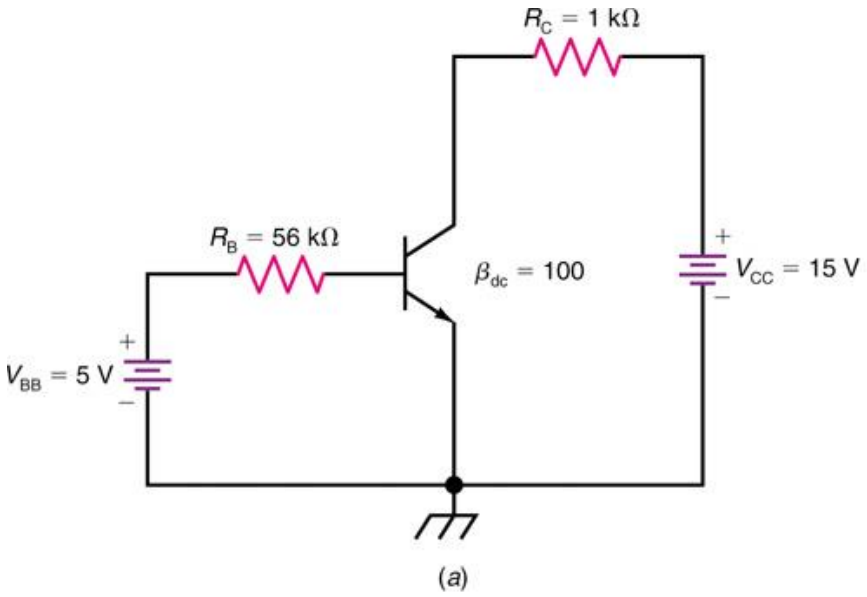


(a) DC biased circuit



Transistor Biasing

- Fig. -1 (a) shows the simplest way to bias a transistor, called **base bias**.
- V_{BB} is the base supply voltage, which is used to forward-bias the base-emitter junction.
- R_B is used to provide the desired value of base current.
- V_{CC} is the collector supply voltage, which provides the reverse-bias voltage required for the collector-base junction.
- The collector resistor, R_C, provides the desired voltage in the collector circuit



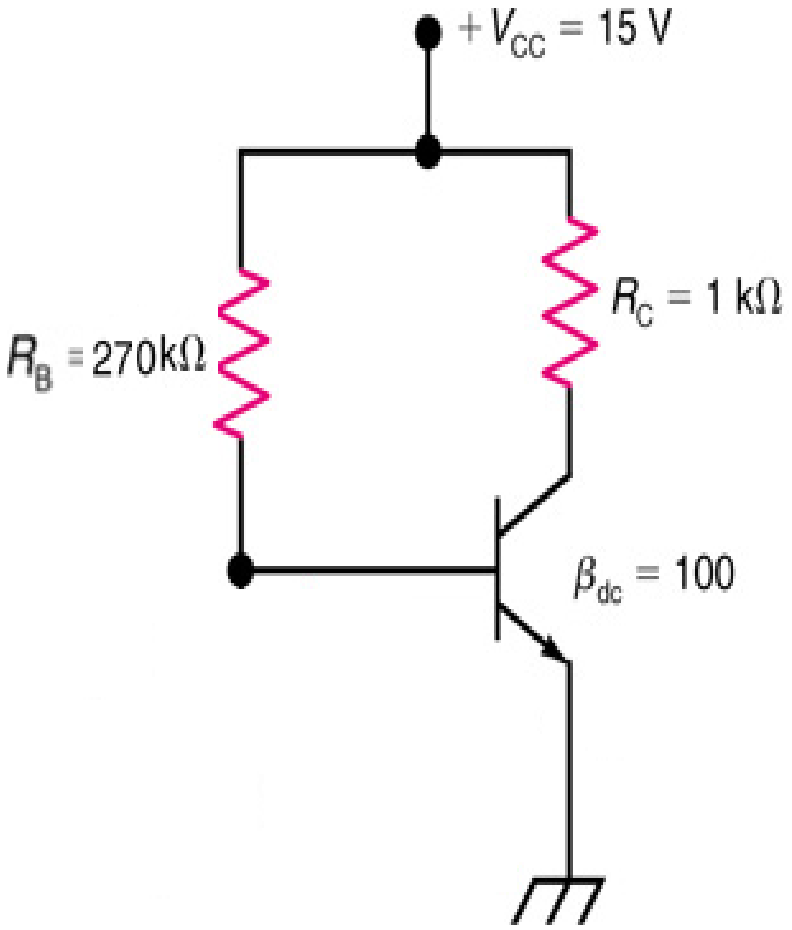
Transistor Biasing: Base Biasing

- A more practical way to provide base bias is to use one power supply.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C \approx \beta_{dc} \times I_B$$

$$V_{CE} \approx V_{CC} - I_C R_C$$



Transistor Biasing

- The **dc load line** is a graph that allows us to determine all possible combinations of I_C and V_{CE} for a given amplifier.

- For every value of collector current, I_C, the corresponding value of V_{CE} can be found by examining the dc load line.

- A sample dc load line is shown in Fig. 1.

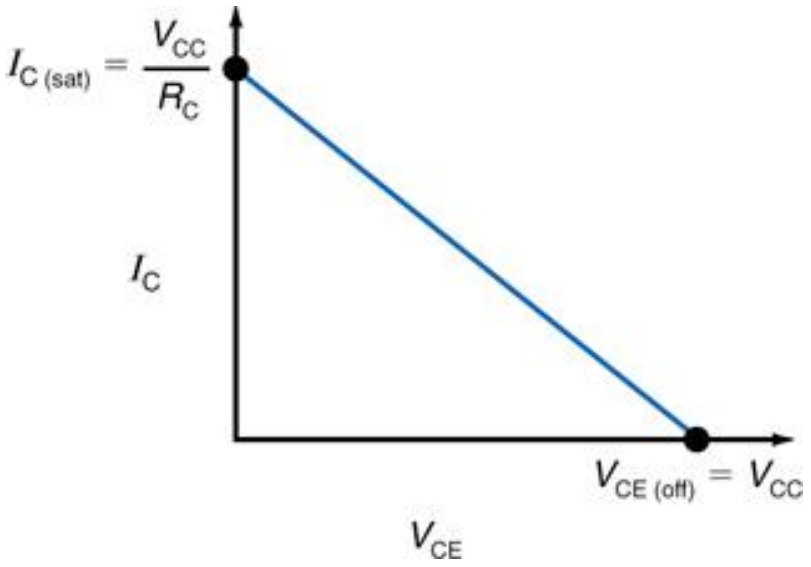


Fig. 1

Transistor Biasing

Midpoint Bias

- Without an ac signal applied to a transistor, specific values of I_C and V_{CE} exist at a specific point on a dc load line
- This specific point is called the Q point (quiescent currents and voltages with no ac input signal)
- An amplifier is biased such that the Q point is near the center of dc load line
  - $I_{CQ} = ½\ I_{C(sat)}$
  - $V_{CEQ} = ½\ V_{CC}$
- Base bias provides a very unstable Q point, because I_C and V_{CE} are greatly affected by any change in the transistor's beta value

Transistor Biasing

Fig. 2 illustrates a **dc load line** showing the end points I_C (sat) and $V_{CE\ (off)}$, as well as the Q point values I_{CQ} and V_{CEQ}.

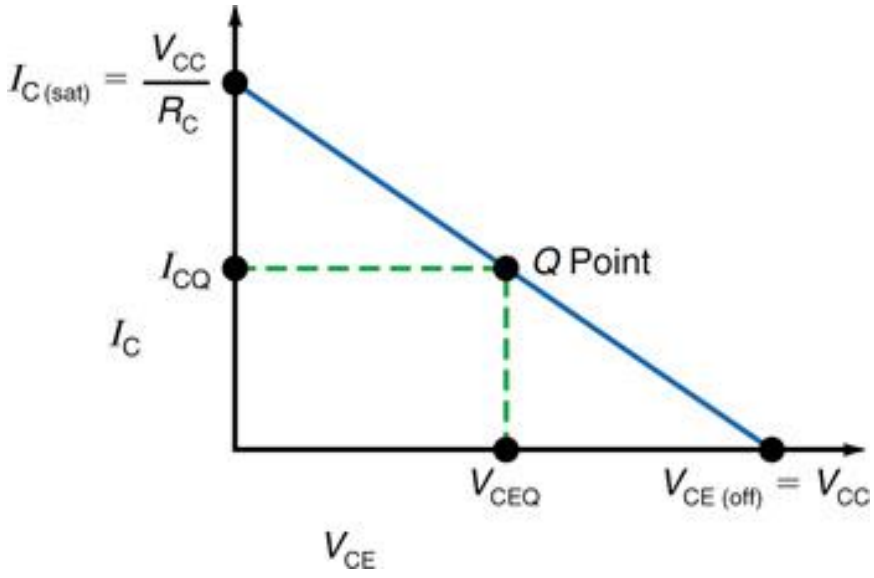
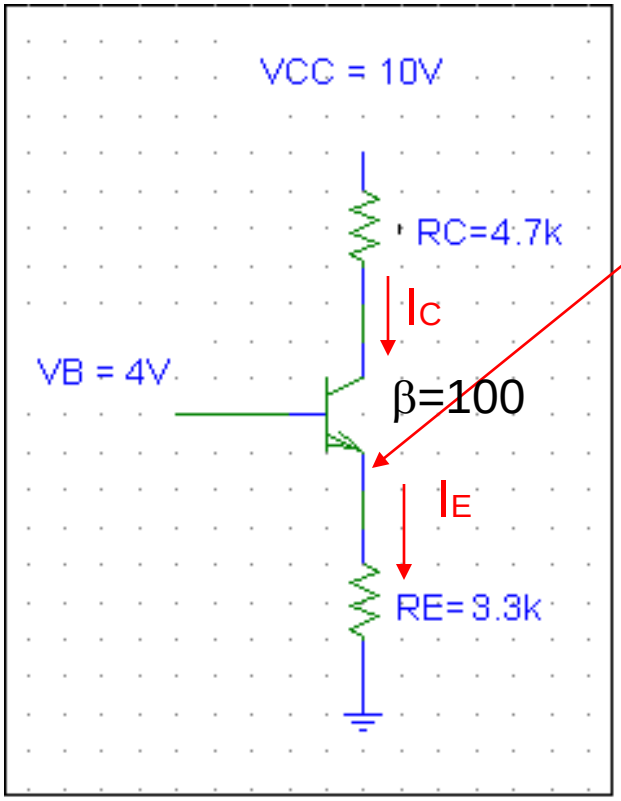


Fig. 2

Analysis of transistor circuits at DC

For all circuits: assume transistor operates in linear region
write B-E voltage loop
write C-E voltage loop



Example

B-E junction acts like a diode

$V_E = V_B - V_{BE} = 4V - 0.7V = 3.3V$

$I_E = (V_E - 0)/R_E = 3.3/3.3K = 1mA$

$I_C \approx I_E = 1mA$

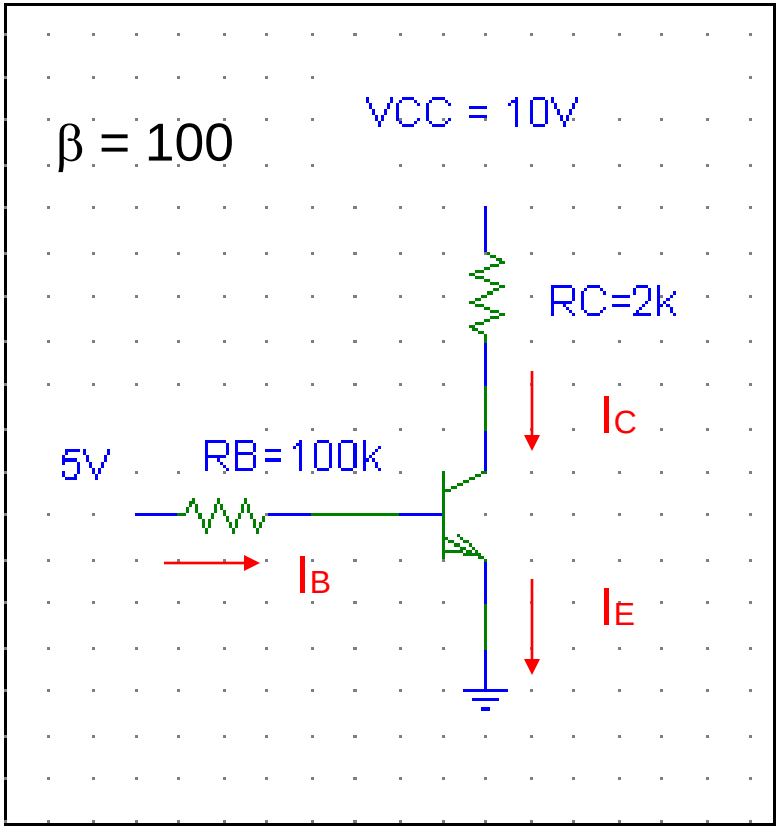
$IB = IC/\beta = 0.01\ mA$

$V_C = 10 - I_C R_C = 10 - 1(4.7) = 5.3V$

$V_{CE} = VC - VE = 5.3 - 3.3\ V = 2V$

Qpoint (2V, 1mA)at 0.01 mA

Example



B-E Voltage loop

$5 = I_B R_B + V_{BE}$, solve for I_B

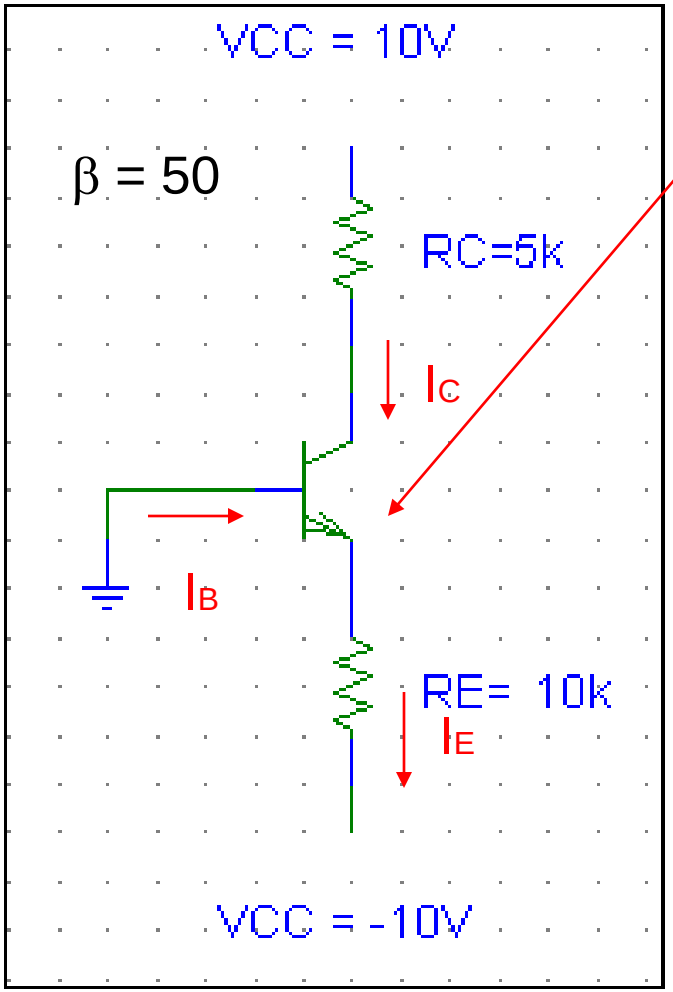
$I_B = (5 - V_{BE})/R_B = (5-.7)/100k = 0.043mA$

$I_C = \beta I_B = (100)0.043mA = 4.3mA$

$V_C = 10 - I_C R_C = 10 - 4.3(2) = 1.4V$

Qpoint (1.4 V, 4.3mA)at I_B =0.043 mA

Exercise



$V_E = 0 - .7 = -0.7V$

$I_E = (V_E - -10)/R_E = (-.7 + 10)/10K = 0.93mA$

$I_C \approx I_E = 0.93mA$

$I_B = I_C/\beta = .93mA/50 = 18.6\mu A$

$V_C = 10 - I_C R_C = 10 - .93(5) = 5.35V$

$V_{CE} = 5.35 - -0.7 = 6.05V$

Qpoint (6.05V, 0.93mA)at 18.6 µA

BIAS STABILITY

❖ Through proper biasing, a desired quiescent operating point of the transistor amplifier in the active region (linear region) of the characteristics is obtained. It is desired that once selected the operating point should remain stable. The maintenance of operating point stable is called Stabilisation.

❖ The selection of a proper quiescent point generally depends on the following factors:

(a) The amplitude of the signal to be handled by the amplifier and distortion level in signal

(b) The load to which the amplifier is to work for a corresponding supply voltage

❖ The operating point of a transistor amplifier shifts mainly with changes in temperature, since the transistor parameters — *β, I_{CO} and V_{BE} (where the symbols carry their usual meaning)—are functions of* temperature.

CALCULATION OF STABILITY FACTORS

❖ **Stability Factor *S*:-** The stability factor *S, as the change of collector current with respect to the reverse saturation* current. keeping β *and* V_{BE} *constant. This can be written as:*

$$S \equiv \frac{\partial I_C}{\partial I_{CO}}$$

❖ **Stability Factor *S'*:-** The variation of I_C *with* V_{BE} *is given by the stability factor S defined by the partial derivative:*

$$S' \equiv \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

❖ **Stability Factor *S"*:-** The variation of I_C *with respect to β is represented by the stability factor, S", given as:*

$$S'' \equiv \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}$$

❖ **General Remarks on Collector Current Stability:-** The stability factors have been defined earlier keeping in mind the change in collector current with respect to changes in I_{CO} , V_{BE} *and β. These stability factors are repeated here for simplicity.*

$$\frac{\Delta I_C}{\Delta_{C1}} = \left(1 + \frac{R_b}{R_e}\right)\frac{M_1 \Delta I_{CO}}{I_{C1}} - \frac{M_1 \Delta V_{BE}}{I_{C1} R_e} + \left(1 + \frac{R_b}{R_e}\right)\frac{M_2 \Delta \beta}{\beta_1 \beta_2}$$

The Thermal Stability of Operating Point (S_{Ico})

❖**Stability Factor *S*:-** The stability factor *S, as the change of collector current with respect to the reverse saturation* current, keeping β *and VBE constant. This can be written as:*

The Thermal Stability Factor : S_{Ico}

$$S=S_{Ico} = \left.\frac{\partial i_C}{\partial I_{C0}}\right|_{V_{BE},\ \beta}$$

This equation signifies that i_C changes S_{Ico} times as fast as I_{CO}

Differentiating the equation of Collector Current $i_C = (1+\beta)Ico + \beta i_B$ & rearranging the terms we can write

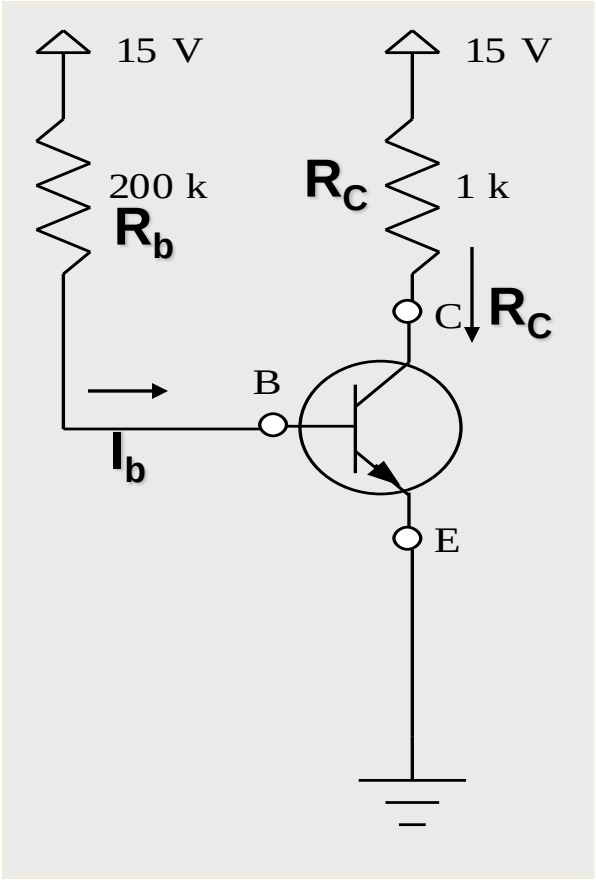
$$S_{Ico} = \frac{1+\beta}{1-\beta\,(\partial i_B/\partial i_C)}$$

It may be noted that Lower is the value of S_{Ico} better is the stability

Various Biasing Circuits

- **Fixed Bias Circuit**
- **Collector to Base Bias Circuit**
- **Fixed Bias with Emitter Resistor**
- **Collector to Base Bias Circuit with Emitter Resistor**
- **Potential Divider Bias Circuit with Emitter Resistor or Self bias**

The Fixed Bias Circuit



The Thermal Stability Factor : S_{Ico}

$$S_{Ico} = \frac{\partial I_c}{\partial I_{co}}\Bigg|_{V_{be},\ \beta}$$

General Equation of S_{Ico} Comes out to be

$$S_{Ico} = \frac{1 + \beta}{1 - \beta\ (\partial I_b / \partial I_C)}$$

Applying KVL through Base Circuit we can write, $I_b R_b + V_{be} = V_{cc}$

Diff w. r. t. I_C, we get $(\partial I_b / \partial I_c) = 0$

$S_{Ico} = (1+\beta)$ is very large

Indicating high un-stability

Merits:

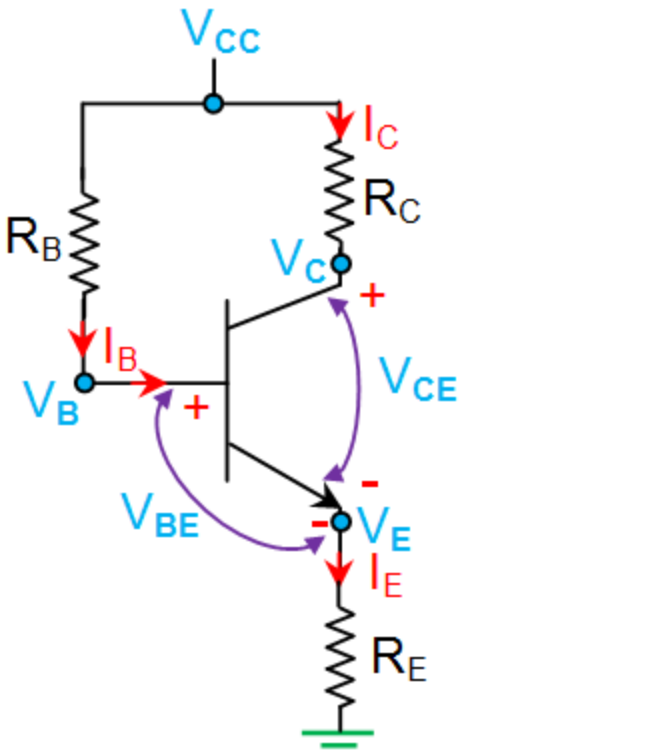
- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

Fixed bias with emitter resistor

The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point.



Fixed Bias with Emitter Resistor

Applying KVL through base circuit

we can write $(I_B + I_C) R_E + I_B R_B + V_{BE} = V_{cc}$

Diff. w. r. t. I_C we get

$$(\partial I_B / \partial I_C) = - R_E / (R_B + R_E)$$

$$\text{Therefore, } S_{Ico} = \frac{(1+\beta)}{1+[\beta R_E/(R_E+R_B)]}$$

Which is less than (1+β), signifying better thermal stability

Merits:

• The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

• As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.

➢ If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.

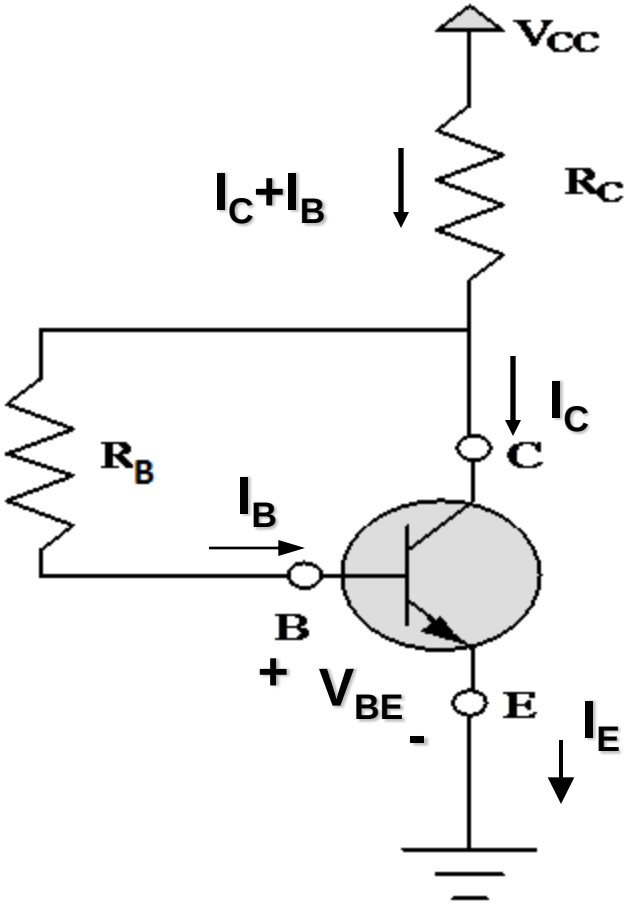
➢ If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.

• In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

Usage:

The feedback also increases the input impedance of the amplifier when seen from the base, which can be advantageous. Due to the above disadvantages, this type of biasing circuit is used only with careful consideration of the trade-offs involved.

The Collector to Base Bias Circuit



This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_F is connected to the collector instead of connecting it to the DC source V_{cc}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

Applying KVL through base circuit

we can write $(I_B + I_C) R_C + I_B R_B + V_{BE} = V_{cc}$

Diff. w. r. t. I_C we get

$$(\partial I_B / \partial I_C) = - R_C / (R_B + R_C)$$

Therefore, $S_{Ico} = \dfrac{(1+\beta)}{1+[\beta R_C/(R_C+R_B)]}$

Which is less than (1+β), signifying better thermal stability

$$\beta R_c \gg R_b.$$

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

• As β -value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_C fairly large or making R_f very low.

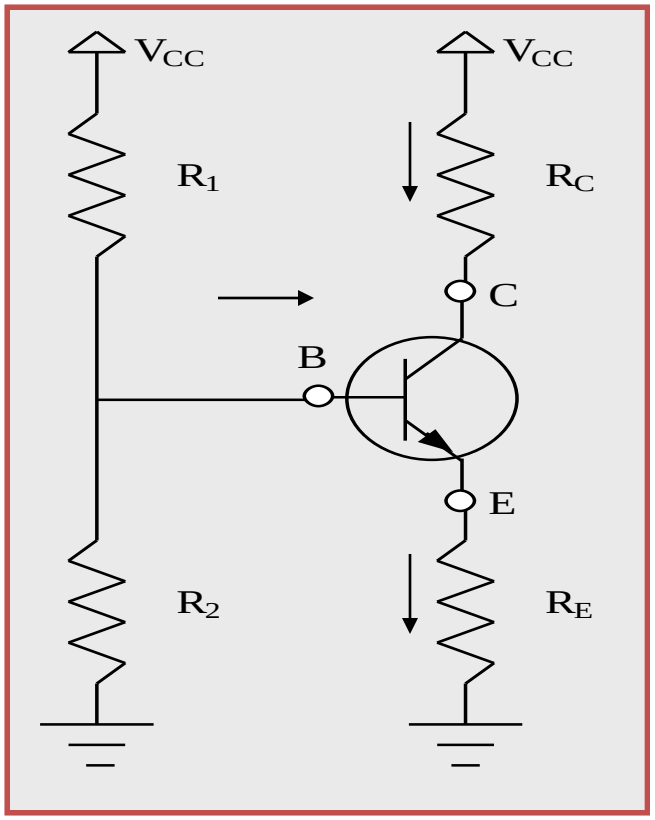
- If R_C is large, a high V_{CC} is necessary, which increases cost as well as precautions necessary while handling.
- If R_B is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_f causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

The Potential Divider Bias Circuit

This is the most commonly used arrangement for biasing as it provide good bias stability. In this arrangement the emitter resistance '$R_{E'}$ provides stabilization. The resistance '$R_{E'}$ cause a voltage drop in a direction so as to reverse bias the emitter junction. Since the emitter-base junction is to be forward biased, the base voltage is obtained from R_1-R_2 network. The net forward bias across the emitter base junction is equal to V_B- dc voltage drop across '$R_{E'}$. The base voltage is set by Vcc and R_1 and R_2. The dc bias circuit is independent of transistor current gain. In case of amplifier, to avoid the loss of ac signal, a capacitor of large capacitance is connected across R_E. The capacitor offers a very small reactance to ac signal and so it passes through the condensor.

The Potential Divider Bias Circuit

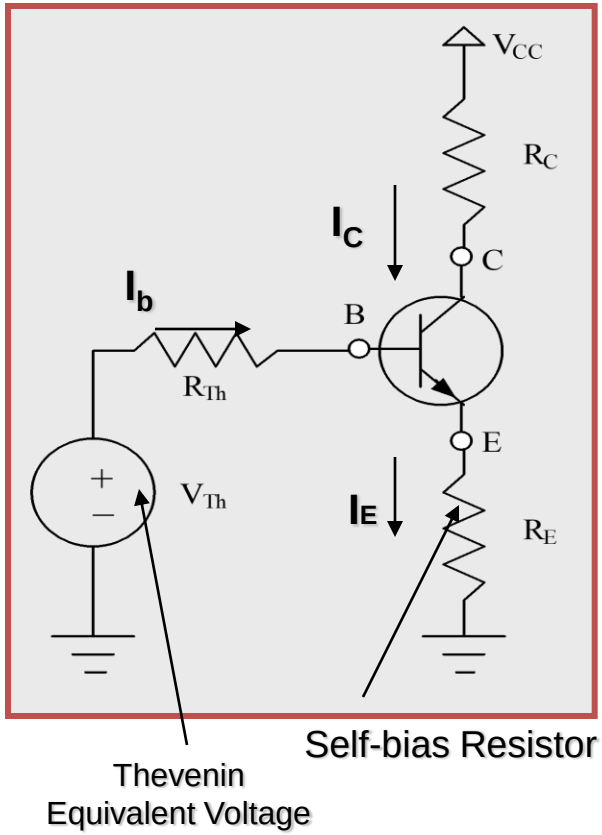


To find the stability of this circuit we have to convert this circuit into its Thevenin's Equivalent circuit

$$R_{th} = \frac{R_1 * R_2}{R_1 + R_2} \quad \& \quad V_{th} = \frac{Vcc\ R_2}{R_1 + R_2}$$

The Potential Divider Bias Circuit

Thevenin Equivalent Ckt



Applying KVL through input base circuit

we can write $I_b R_{Th} + I_E R_E + V_{be} = V_{Th}$

Therefore, $I_b R_{Th} + (I_C + I_b) R_E + V_{BE} = V_{Th}$

Diff. w. r. t. I_C & rearranging we get

$$(\partial I_b / \partial I_c) = - R_E / (R_{Th} + R_E)$$

Therefore,

$$S_{Ico} = \frac{1+\beta}{1+\left[\beta \frac{R_E}{R_E + R_{Th}}\right]}$$

This shows that S_{Ico} is inversely proportional to R_E and It is less than (1+β), signifying better thermal stability

Merits:

- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making R1||R2 very low.
  - If R_E is of large value, high V_{CC} is necessary. This increases cost as well

  as precautions necessary while handling.
  - If R1 || R2 is low, either R1 is low, or R2 is low, or both are low. A low R1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R2 lowers Vbe, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
  - AC as well as DC feedback is caused by RE, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

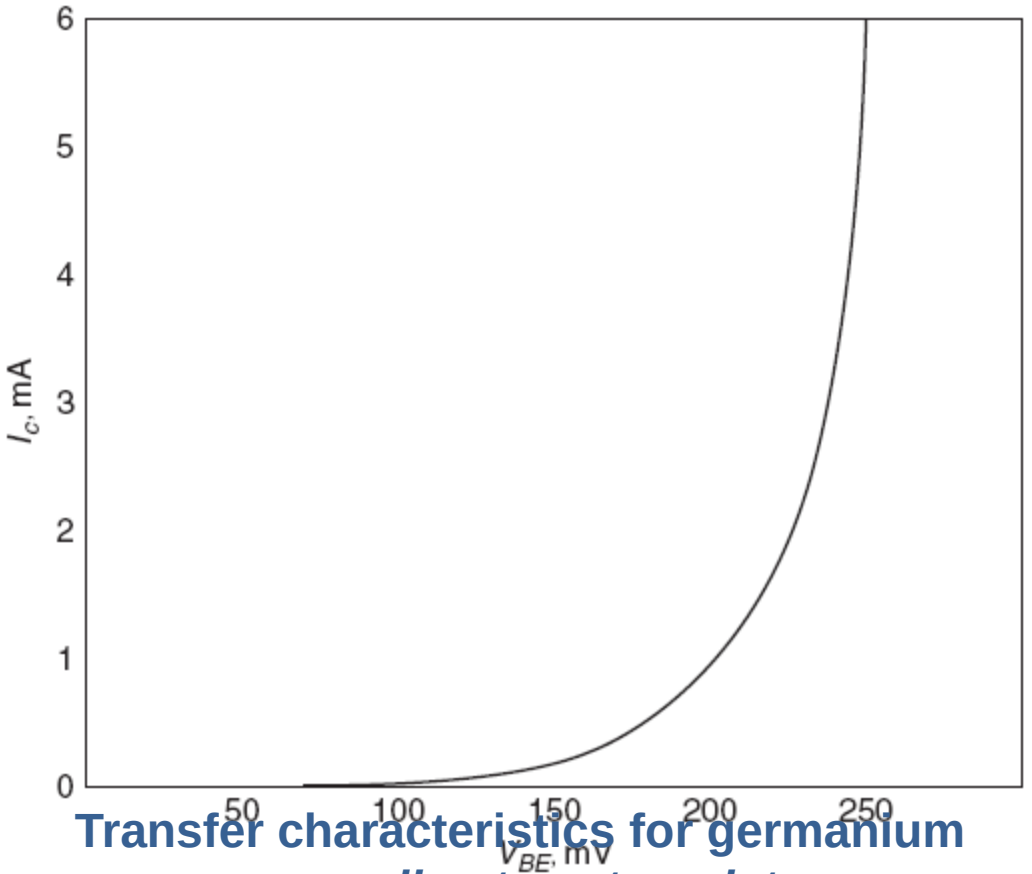
Usage:

The circuit's stability and merits as above make it widely used for linear circuits.

BIASING AND BIAS STABILITY

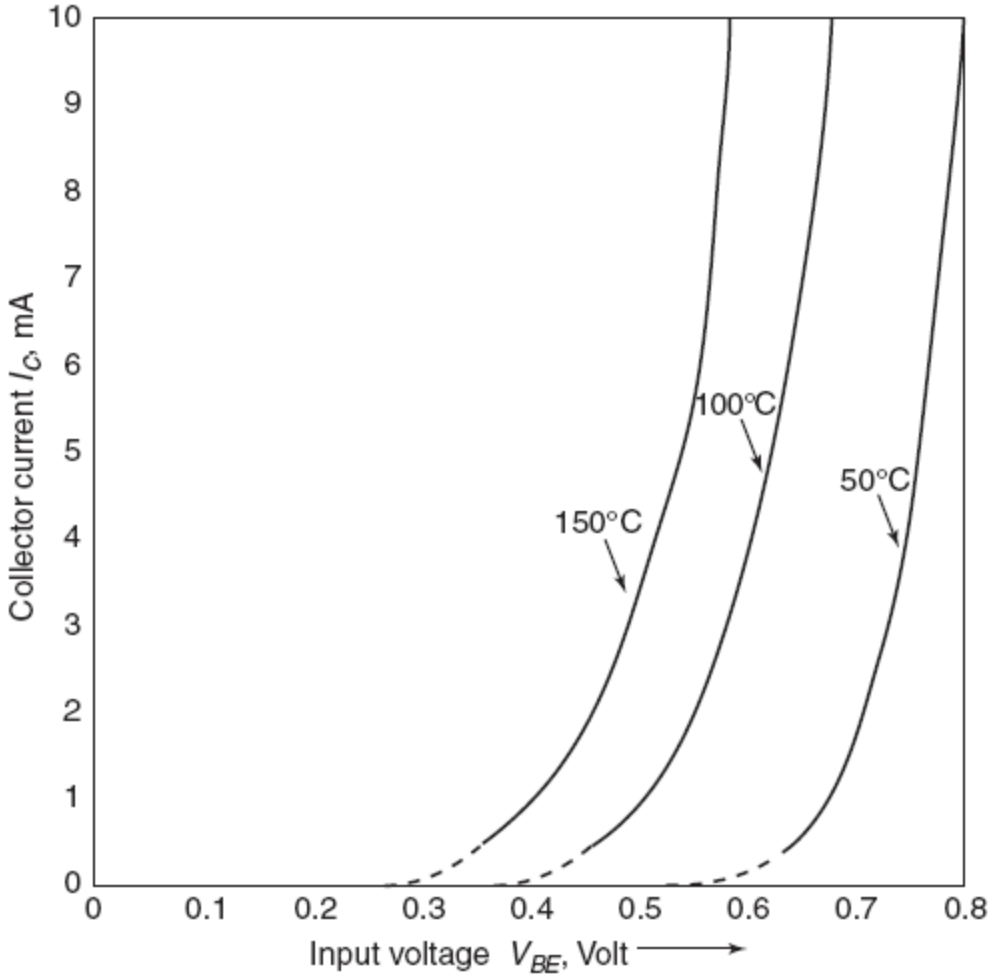
❖ **Stabilization Against Variations in *ICO, VBE , and β***

➢**Transfer characteristic:-** In this particular characteristic, the output current I_C *is a function of input voltage for* the germanium transistor. Thus, the word “transfer” is used for this characteristic.

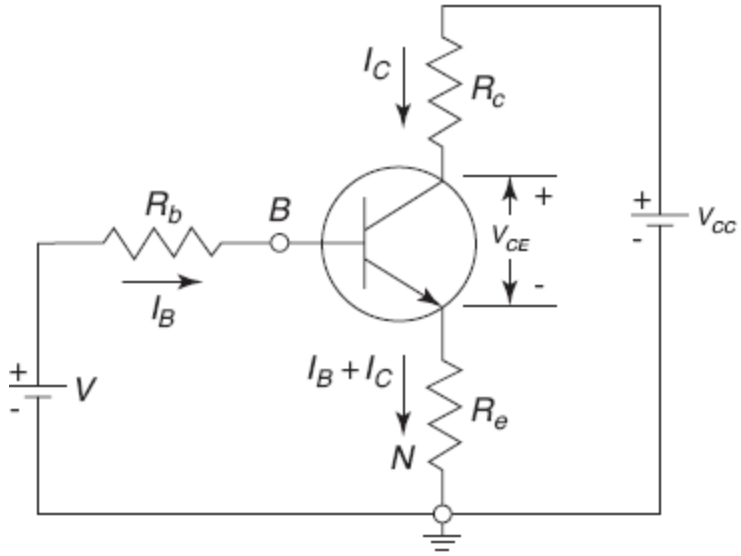


Transfer characteristics for germanium *p–n–p alloy type transistor*

BIASING AND BIAS STABILITY

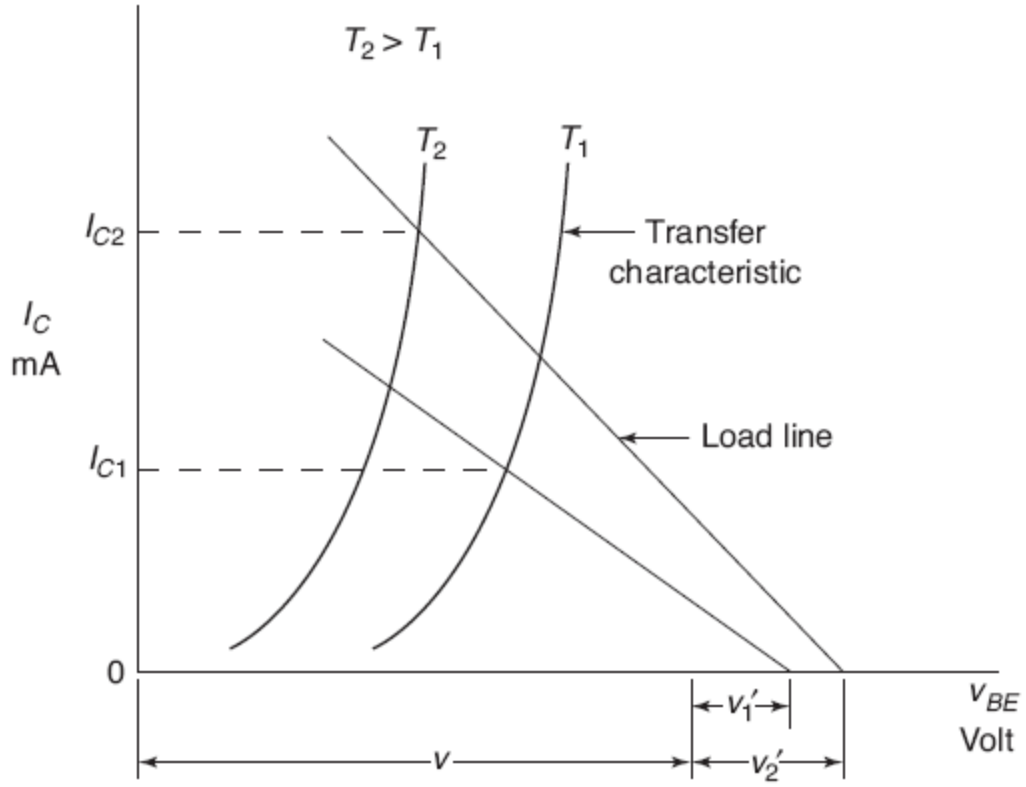


Collector current vs. base-to-emitter voltage for a silicon transistor



Self-bias circuit

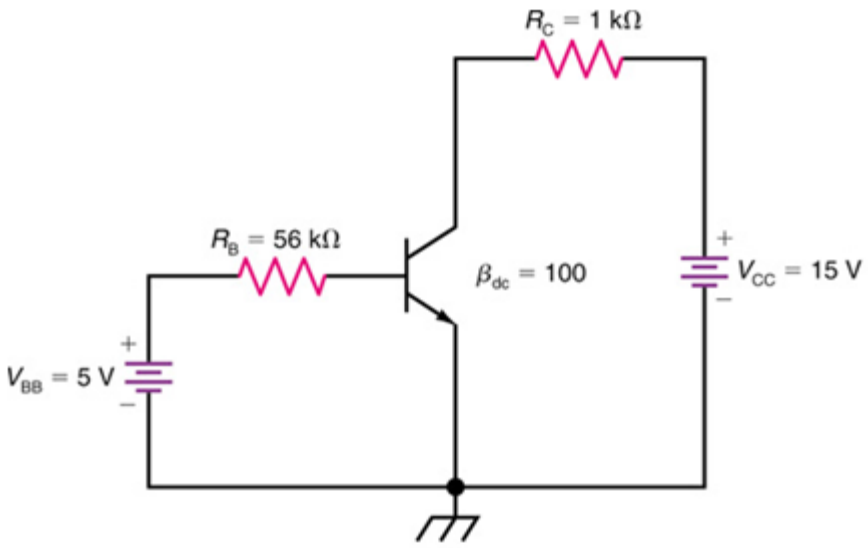
BIASING AND BIAS STABILITY



Variation of the collector current with temperature because of *VBE, ICO and β*

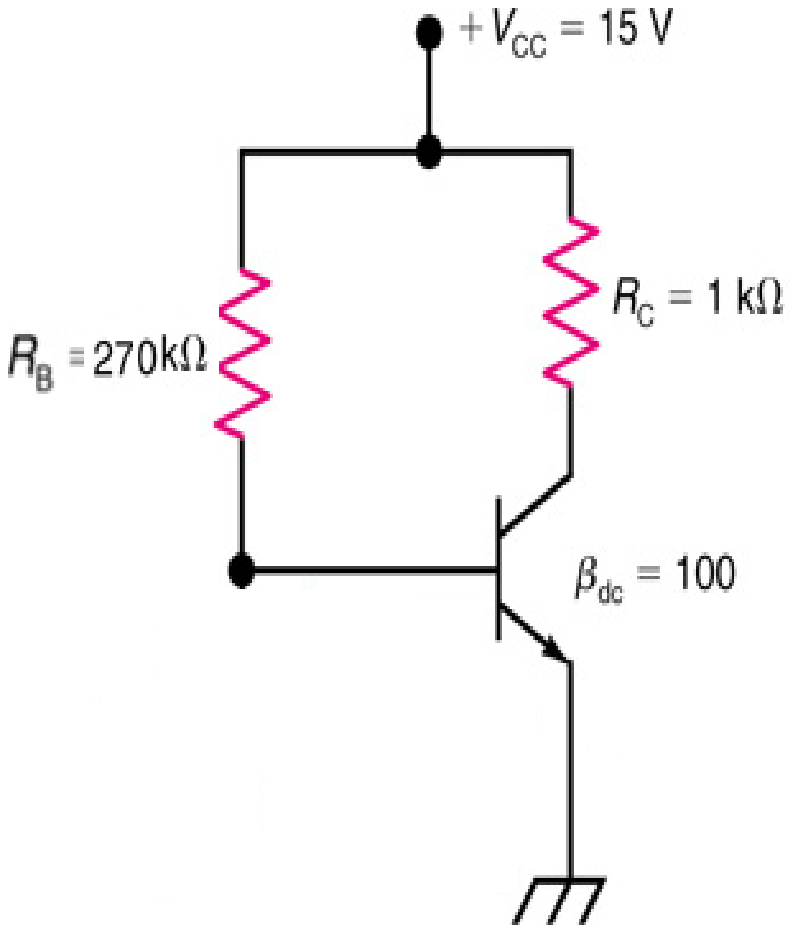
Base Bias – Example 1

- Solve for I_B, I_C and V_{CE}
- Construct a dc load line showing the values of $I_{C(sat)}$, $V_{CE(off)}$, I_{CQ} and V_{CEQ}



Base Bias – Example 2

- Solve for I_B, I_C and V_{CE}
- Construct a dc load line showing the values of $I_{C(sat)}$, $V_{CE(off)}$, I_{CQ} and V_{CEQ}

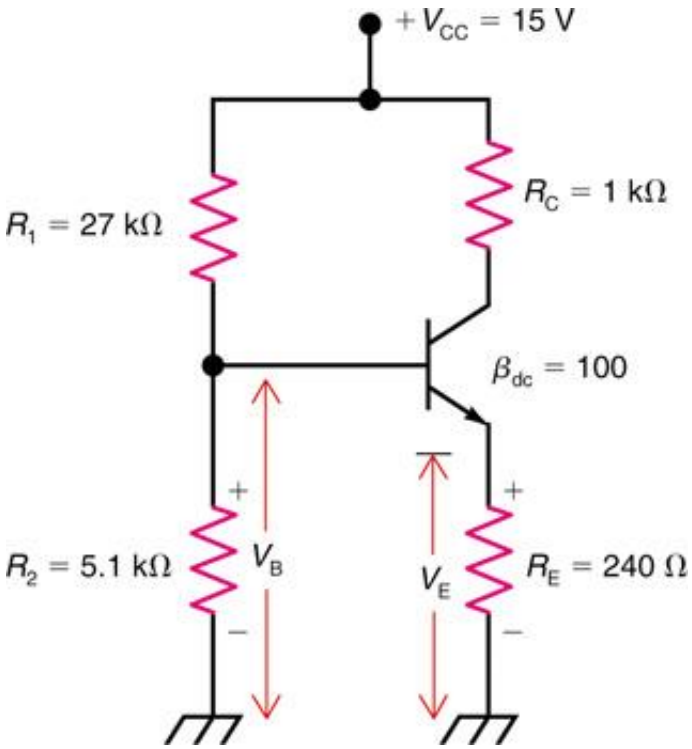


Excercise

- The most popular way to bias a transistor is with **voltage-divider bias**.

- The advantage of voltage-divider bias lies in its stability.

- An example of voltage-divider bias is shown in Fig..



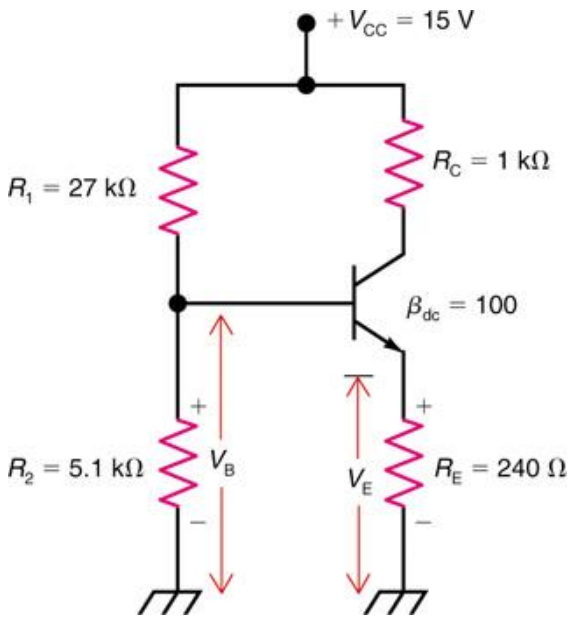
$$V_B = \frac{R_2}{R_1 + R_2} \; X \; V_{CC}$$

$$V_E = V_B - V_{BE}$$

$$I_E \approx I_C$$

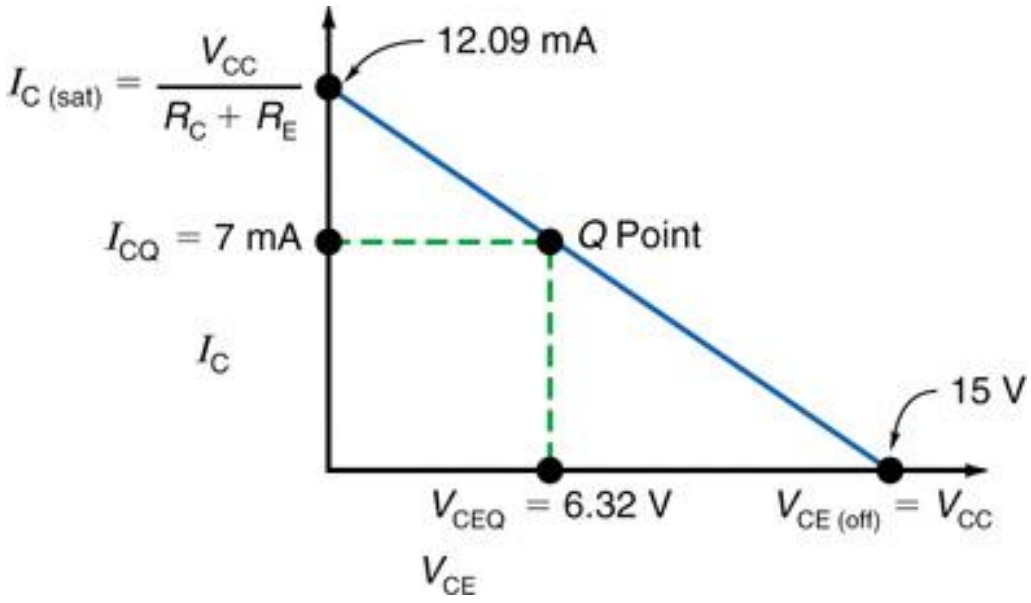
Voltage Divider Bias – Example

- Solve for V_B, V_E, I_E, I_C, V_C and V_{CE}
- Construct a dc load line showing the values of $I_{C(sat)}$, $V_{CE(off)}$, I_{CQ} and V_{CEQ}



solution

- Fig. shows the **dc load line** for voltage-divider biased transistor circuit in.
- End points and Q points are
  - I_C (sat) = 12.09 mA
  - V_{CE} (off) = 15 V
  - I_{CQ} = 7 mA
  - V_{CEQ} = 6.32 V



Excercise

- Both positive and negative power supplies are available

- **Emitter bias** provides a solid Q point that fluctuates very little with temperature variation and transistor replacement.

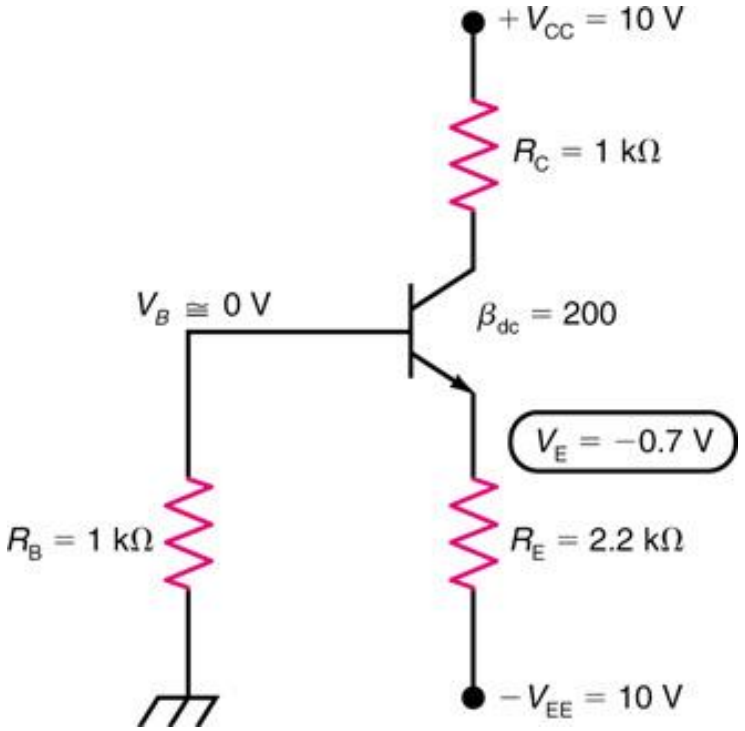
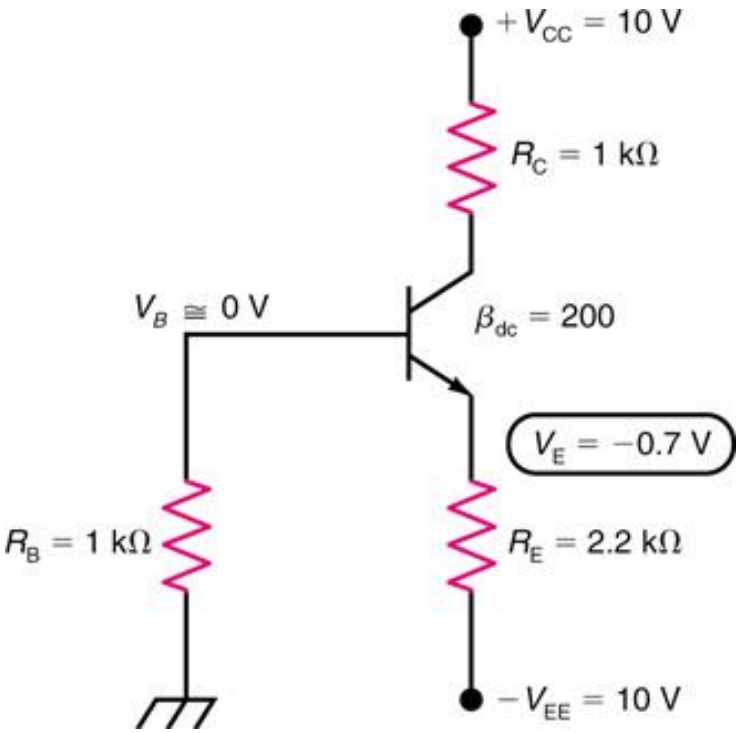


Fig.

Emitter Bias – Example

- Solve for I_E, and V_C



Thermal Runaway

The maximum average power $P_{D(max)}$ which a transistor can dissipate depends upon the transistor construction and may lie in the range from a few milliwatts to 200 W. As mentioned earlier, the power dissipated within a transistor is predominantly the power dissipated at its collector base junction. Thus maximum power is limited by the temperature that the collector-base junction can withstand. For silicon transistor this temperature is in the range 150 to 225 °C, and for germanium it is between 60 to 100 °C. The collector-base junction temperature may rise because of two reasons :

- Due to rise in ambient temperature
- Due to self heating.

The self heating can be explained as follows :

The increase in the collector current increases the power dissipated at the collector junction. This, in turn further increases the temperature of the junction and hence increase in the collector current. The process is cumulative and it is referred to as **self heating**. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called '**Thermal runaway**' of the transistor.

Thermal Resistance

The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction. It is given as

$$\partial T = T_j - T_A = \theta P_D \quad \ldots (1)$$

The Condition for Thermal Stability

As we know, the thermal runaway may even burn and destroy the transistor, it is necessary to avoid thermal runaway. The required condition to avoid thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated. It is given by,

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad \ldots (3)$$

If we differentiate equation (1)

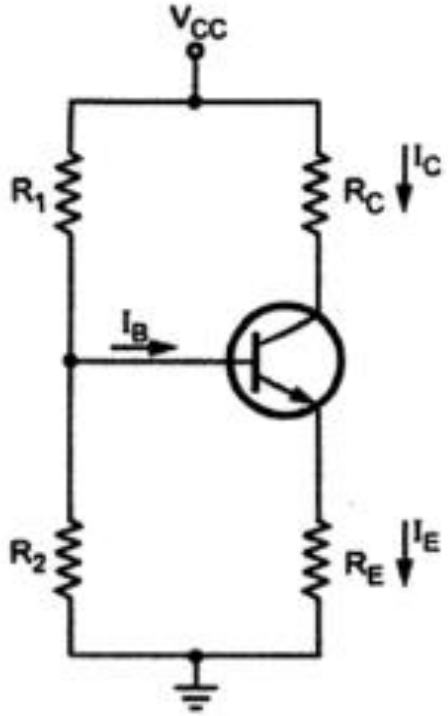
$T_j - T_A = \theta P_D$ with respect to T_j we get,

$$1 = \theta \frac{\partial P_D}{\partial T_j}$$

$$\therefore \quad \frac{\partial P_D}{\partial T_j} = \frac{1}{\theta} \quad \ldots (4)$$

Now substituting equation (4) in equation (3) we get

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta} \quad \ldots (5)$$



This condition must be satisfied to prevent thermal runaway. By proper design of biasing circuit it is possible to ensure that the transistor cannot runaway below a specified ambient temperature or even under any condition.

Let us consider voltage divider bias circuit for the analysis.

From the Fig. 1.73 we can say that,

P_C = Heat generated at the collector junction

= D.C. Power input to the circuit – The power lost as I^2R in R_C and R_E

$$P_C = V_{CC} \times I_C - I_C^2 R_C - I_E^2 R_E \quad \ldots (6)$$

If we consider $I_C \cong I_E$ we get

$$P_C = V_{CC} \times I_C - I_C^2 (R_C + R_E) \quad \ldots (7)$$

Differentiating equation (7) with respect to I_C we get

As the reverse saturation current for both silicon and germanium increases about 7 percent per °C, we can write

$$\frac{\partial I_{CO}}{\partial T_j} = 0.07\, I_{CO} \qquad \ldots (12)$$

Now substituting value of $\frac{\partial I_C}{\partial T_j}$ and $\frac{\partial P_C}{\partial I_C}$ in equation (11) we get,

$$\frac{\partial I_C}{\partial T_j} = S \times 0.07\, I_{CO} \qquad \ldots (13)$$

Now substituting value of $\frac{\partial I_C}{\partial T_j}$ and $\frac{\partial P_C}{\partial I_C}$ from equations (13) and (8) into equation (9) we get,

$$[V_{CC} - 2\, I_C\, (R_C + R_E)]\, (S)\, (0.07\, I_{CO}) < \frac{1}{\theta} \qquad \ldots (14)$$

As S, I_{CO} and θ are positive, we see that the inequality in equation (14) is always satisfied provided that the quantity in the square bracket is negative.

$$\therefore \quad V_{CC} < 2 I_C (R_C + R_E)$$

$$\therefore \quad \frac{V_{CC}}{2} < I_C (R_C + R_E) \qquad \ldots (15)$$

Applying KVL to the collector circuit of Fig. 1.73 we get,

$$V_{CE} = V_{CC} - I_C (R_E + R_C) \quad \because \quad I_C \cong I_E$$

$$\therefore \quad I_C (R_E + R_C) = V_{CC} - V_{CE}$$

Substituting value of $I_C (R_E + R_C)$ in equation (15) we get,

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$\therefore \quad V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

$$\therefore \quad V_{CE} < \frac{V_{CC}}{2}$$

Thus if $V_{CE} < \frac{V_{CC}}{2}$, the stability is ensured. But in transformer coupled circuit, R_C and R_E are quite small and $V_{CE} \cong V_{CC}$. Hence it is necessary to design transformer coupled circuits with stability factor as close to 1 as possible to avoid thermal runaway.

Diode Compensation Techniques

Compensation for V_{BE} :

a) Diode in Emitter Circuit

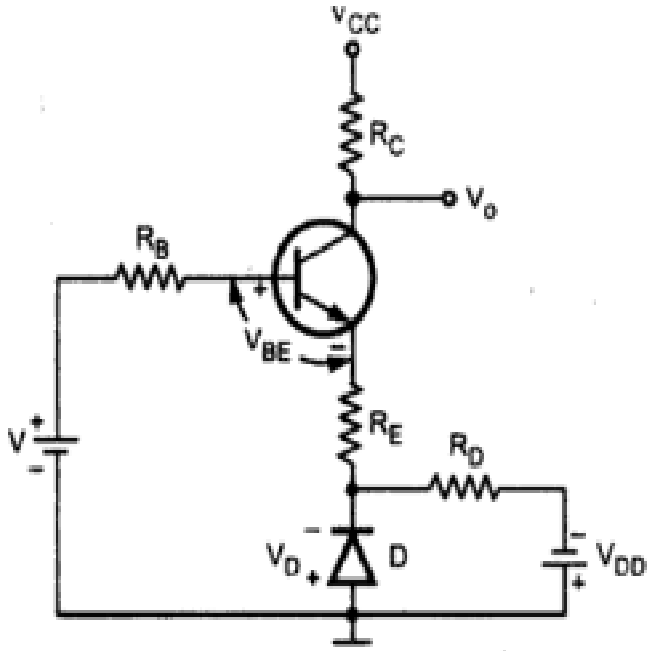


Fig. Stabilization by means of voltage divider bias and diode compensation technique

Fig. shows the voltage divider bias with bias compensation technique.

Here, separate supply V_{DD} is used to keep diode in forward biased condition. If the diode used in the circuit is of same material and type as the transistor, the voltage across the diode will have the same temperature coefficient ($-2.5\,mV/°C$) as the base to emitter voltage V_{BE}. So when V_{BE} changes by ∂V_{BE} with change in temperature, V_D changes by ∂V_D and

$\partial V_D' \approx \partial V_{BE}$, the changes tend to cancel each other.

We know,

$$V_{BE} = V_T \frac{[R_B + (1+\beta)R_E]}{\beta} I_C + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

$$\therefore \quad \frac{[R_B + (1+\beta)R_E]}{\beta} I_C = V_T - V_{BE} + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

$$\therefore \quad I_C = \frac{\beta[V_T - V_{BE}] + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E} \quad \ldots (1)$$

If we write KVL to the base circuit of the Fig. 1.36, then equation 1 becomes

$$I_C = \frac{\beta[V - (V_{BE} - V_D)] + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E} \quad \ldots (2)$$

Since V_D tracks V_{BE} with respect to temperature, it is clear from equation (2) that I_C will be insensitive to variations in V_{BE}.

Compensation for I_{CO}

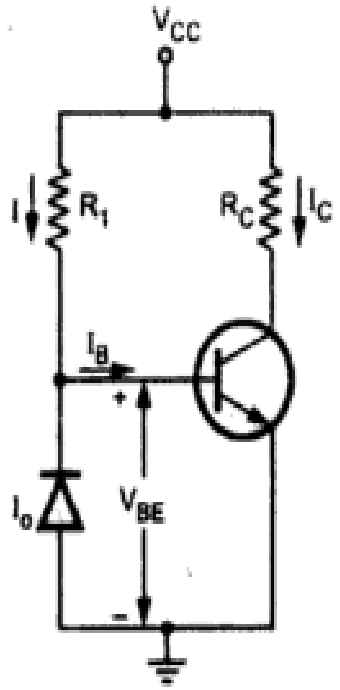


Fig. Diode compensation for a germanium transistor

In case of germanium transistors, changes in I_{CO} with temperature are comparatively larger than silicon transistor. Thus, in germanium transistor changes in I_{CO} with temperature play the more important role in collector current stability than the changes in the V_{BE}. The Fig shows diode compensation technique commonly used for stabilizing germanium transistors. It offers stabilization against variation in I_{CO}. In this circuit diode is kept in reverse biased condition. In reverse biased condition the current flowing through diode is only the leakage current. If the diode and the transistor are of the same type and material, the leakage current I_O of the diode will increase with temperature at the same rate as the collector leakage current I_{CO}.

Thermistor Compensation

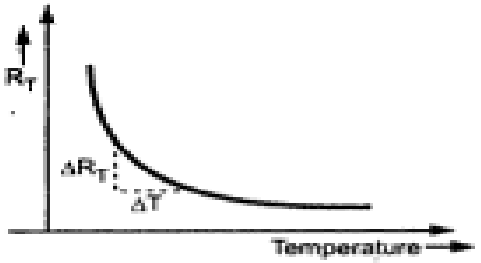


Fig. Temperature Vs R_T resistance of thermistor

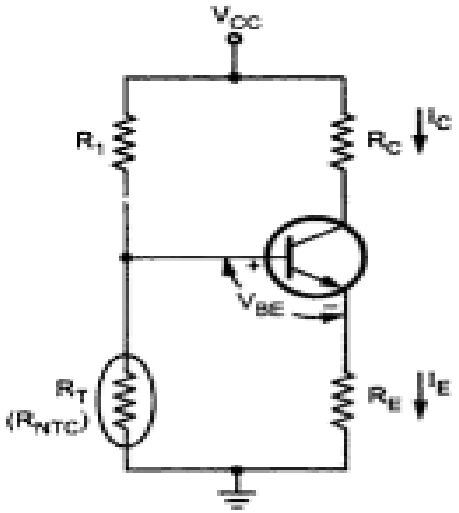


Fig. (a) Thermistor compensation technique

This method of transistor compensation uses temperature sensitive resistive elements, thermistors rather than diodes or transistors. It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature as shown in the Fig. 1.36.

$$\text{Slope of this curve} = \frac{\partial R_T}{\partial T}$$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor, and the slope is negative. So we can say that thermistor has negative temperature coefficient of resistance (NTC). Fig. (a) shows thermistor compensation technique. As shown in Fig. 1.37 (a), R_2 is replaced by thermistor R_T in self bias circuit. With increase in temperature, R_T decreases. Hence voltage drop across it also decreases. This voltage drop is nothing but the voltage at the base with respect to ground. Hence, V_{BE} decreases which reduces I_B. This behaviour will tend to offset the increase in collector current with temperature.

We know, $I_C = \beta I_B + (1+\beta) I_{CBO}$

In this equation, there is increase in I_{CBO} and decrease in I_B which keeps I_C almost constant.

Sensistor Compensation Technique

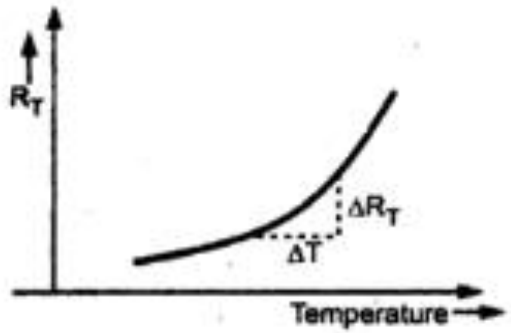
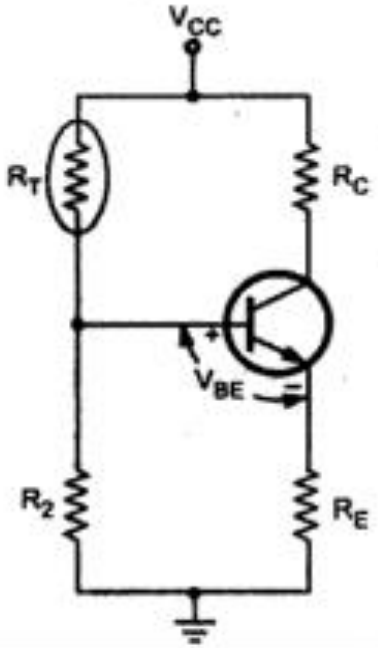


Fig. 1 Temperature Vs resistance of sensistor, R_T



This method of transistor compensation uses temperature sensitive resistive element, sensistors rather than diodes or transistors. It has a positive temperature coefficient, its resistance increases exponentially with increasing temperature as shown in the Fig. 1 .

$$\text{Slope of this curve} = \frac{\partial R_T}{\partial T}$$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor, and the slope is positive.

So we can say that sensistor has positive temperature coefficient of resistance (PTC).

Fig. shows sensistor compensation technique.

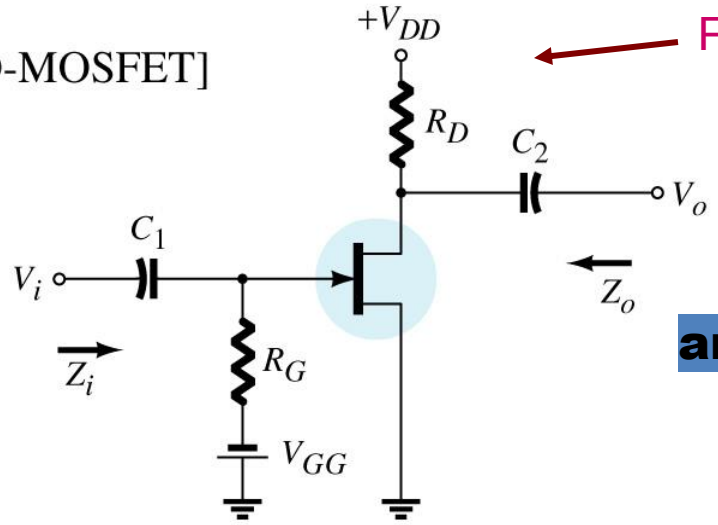
As shown in Fig. 1.39, R_1 is replaced by sensistor R_T in self bias circuit. Now, R_T and R_2 are the two resistors of the potential divider.

Biasing Circuits used for JFET

- Fixed bias circuit
- Self bias circuit
- Potential Divider bias circuit

JFET (n-channel) Biasing Circuits

Fixed-bias
[JFET or D-MOSFET]



For Fixed Bias Circuit

Applying KVL to gate circuit we get

$$V_{GG} = I_G R_G + V_{GS} = V_{GS} = Fixed\ ,\because I_G = 0$$

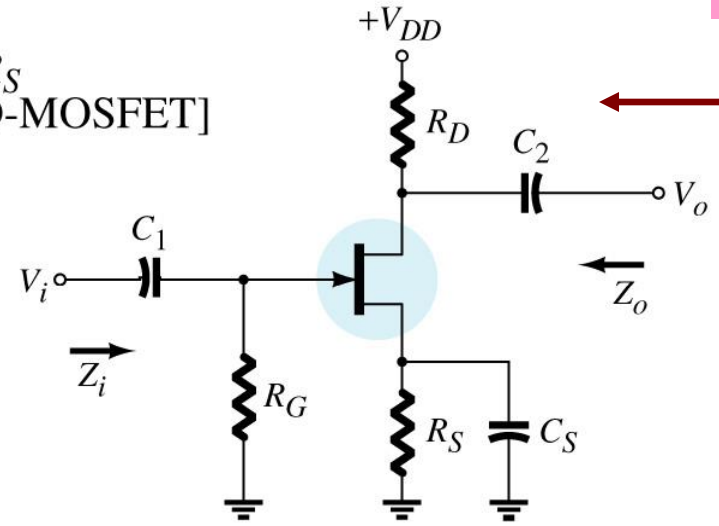
and

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\text{and } V_{DS} = V_{DD} - I_{DS}R_D$$

Where, $V_p = V_{GS\text{-}off}$ & I_{DSS} is Short ckt. I_{DS}

Self-bias
bypassed R_S
[JFET or D-MOSFET]



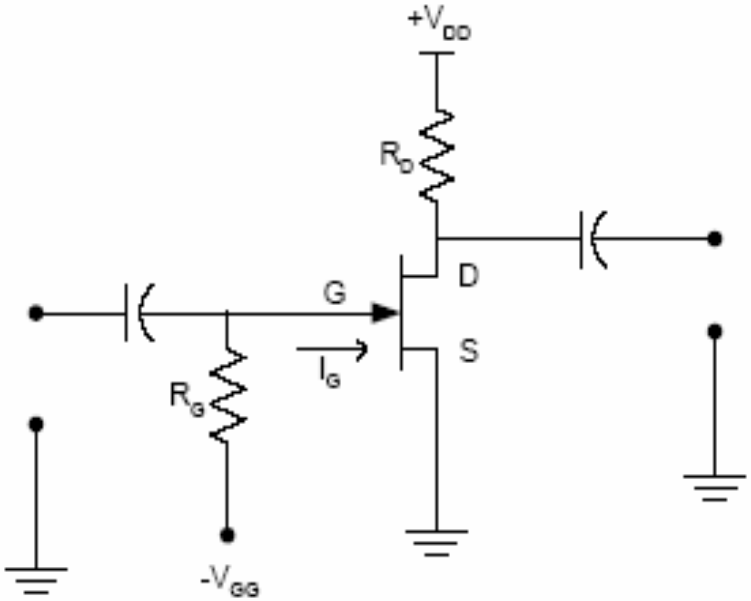
For Self Bias Circuit

$$V_{GS} + I_{DS}R_S = 0$$

$$\therefore I_{DS} = -\frac{V_{GS}}{R_S}$$

JFET Biasing Circuits Count…

Gate Bias: or Fixed Bias Ckt.



Since $I_G = 0$,

$$V_{GS} = V_{GG}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

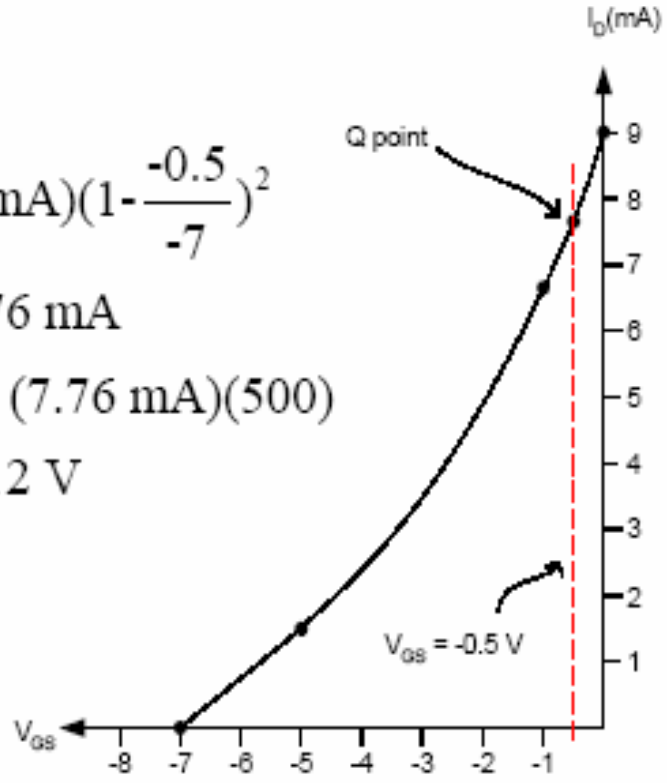
- Example: Determine the Q-point values for the gate biasing circuit if $V_{GG} = -0.5$ V, $V_{GS(off)} = -7$ V, $I_{DSS} = 9$ mA, $V_{DD} = 5$ V and $R_D = 500\Omega$.

$$I_D = (9\text{mA})\left(1 - \frac{-0.5}{-7}\right)^2$$

$$= 7.76 \text{ mA}$$

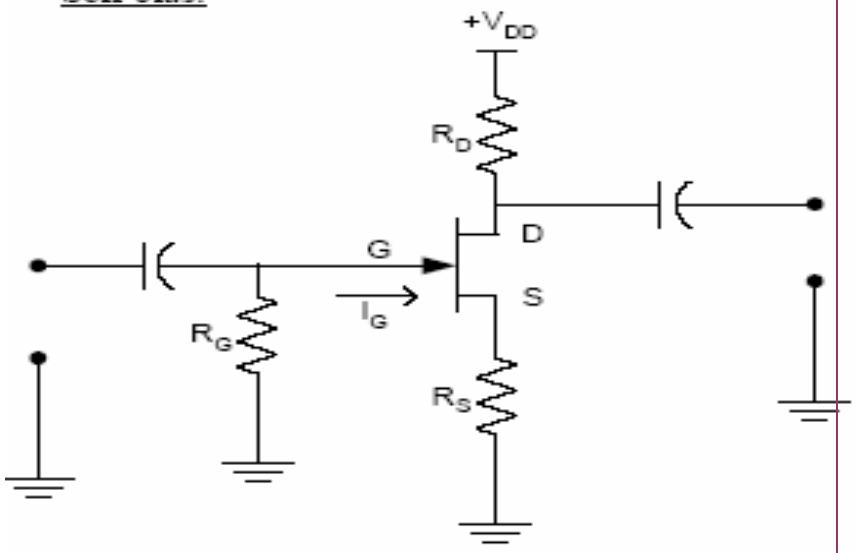
$$V_{DS} = 5 - (7.76 \text{ mA})(500)$$

$$= 1.12 \text{ V}$$



JFET Self (or Source) Bias Circuit

Self bias:



Since $I_G = 0$, $V_G = 0$

$V_S = I_D R_S$

$V_{GS} = -I_D R_S$

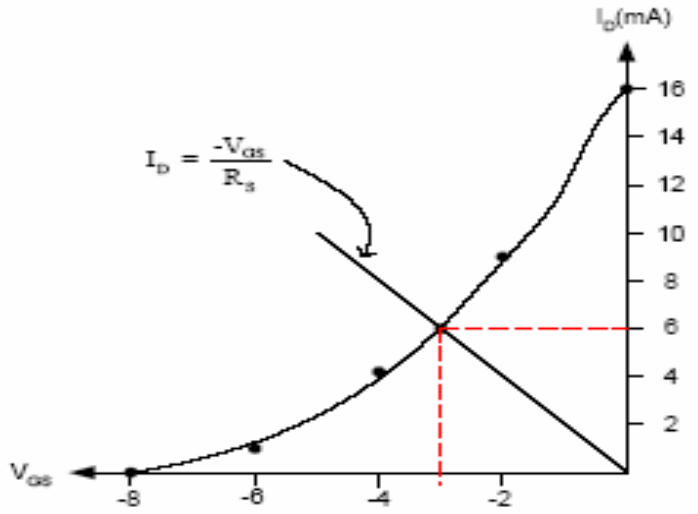
$$I_D = \frac{-V_{GS}}{R_S}$$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$$\text{and } I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\therefore I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = -\frac{V_{GS}}{R_S}$$

- Example: Determine the Q-point values for the self biasing circuit if $V_{GS(off)} = -8$ V , $I_{DSS} = 16$ mA , $V_{DD} = 10$ V , $R_D = 500\ \Omega$, $R_G = 1$ MΩ and $R_S = 500\ \Omega$.



$I_D = 6$ mA

$V_{DS} = 10 - (6\text{mA})(500+500)$

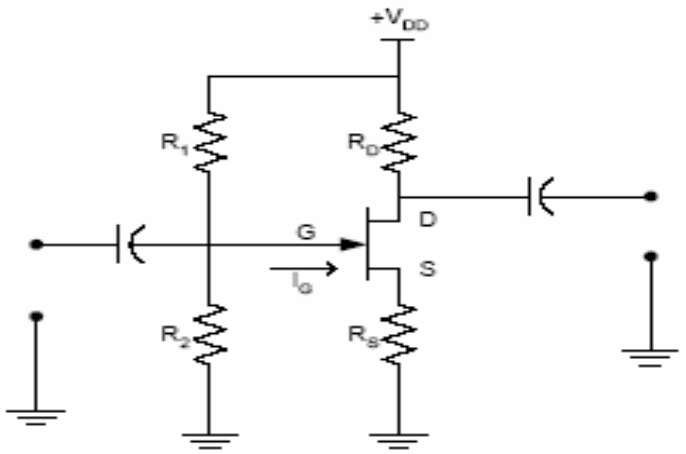
$= 4$ V

$$I_{DSS}\left[1 - 2\frac{V_{GS}}{V_P} + \left(\frac{V_{GS}}{V_P}\right)^2\right] + \frac{V_{GS}}{R_S} = 0$$

This quadratic equation can be solved for V_{GS} & I_{DS}

The Potential (Voltage) Divider Bias

Voltage-divider bias:



Since $I_G = 0$,

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$

The method used to plot the dc bias line for the voltage-divider bias is as follows:

1. Plot the transconductance curve for the specific JFET.
2. Calculate V_G.
3. Plot V_G on the positive x-axis.
4. Solve for I_D using
$$I_D = \frac{V_G}{R_S}$$
5. Plot I_D found in (4) on the y-axis.
6. Extend the line to intersect the transconductance curve to obtain the Q-point values.

$$\therefore I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 - \frac{V_G - V_{GS}}{R_S} = 0$$

Solving this quadratic equation gives V_{GS} *and* I_{DS}

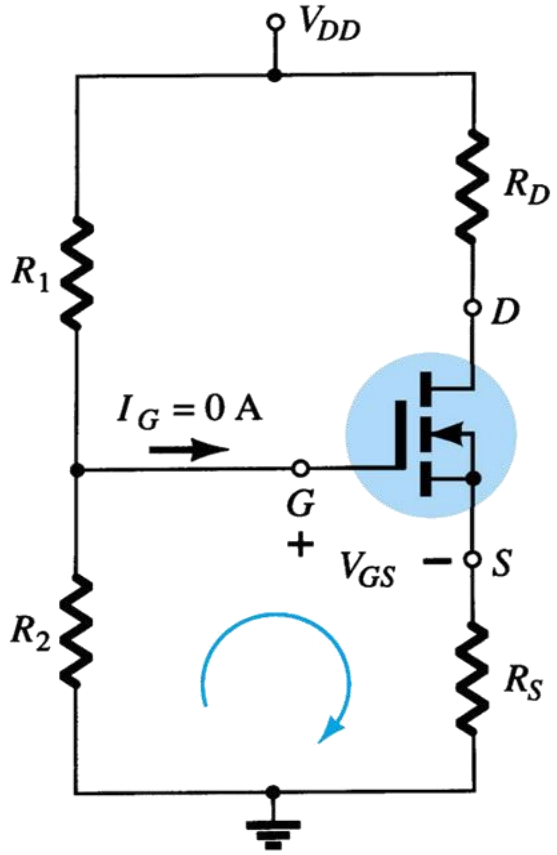
DC analysis step for Feedback Biasing Enhancement type MOSFET

- Find k using the datasheet or specification given;

  ex: $V_{GS(ON)}$,$V_{GS(TH)}$
- Plot transfer characteristics using the formula

  $I_D=k(V_{GS} – V_T)^2$. Three point already defined that is $I_{D(ON)}$, $V_{GS(ON)}$ and $V_{GS(TH)}$
- Plot a point that is slightly greater than V_{GS}
- Plot the linear characteristics (network bias line)
- The intersection defines the Q-point

Voltage-Divider Biasing



Again plot the line and the transfer curve to find the Q-point.
Using the following equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Input loop : $V_{GS} = V_G - I_D R_S$

Output loop : $V_{DS} = V_{DD} - I_D (R_S + R_D)$