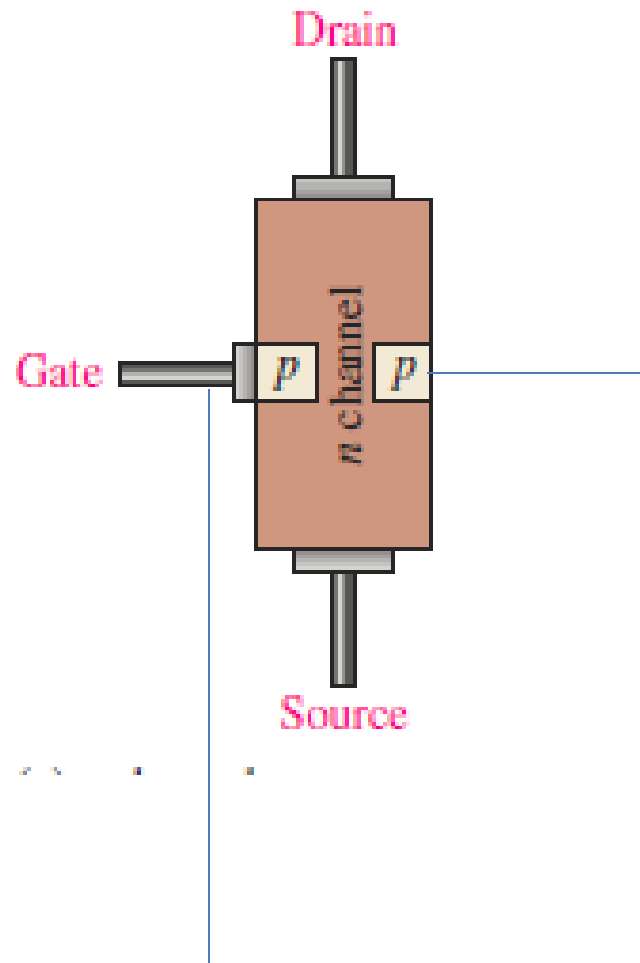
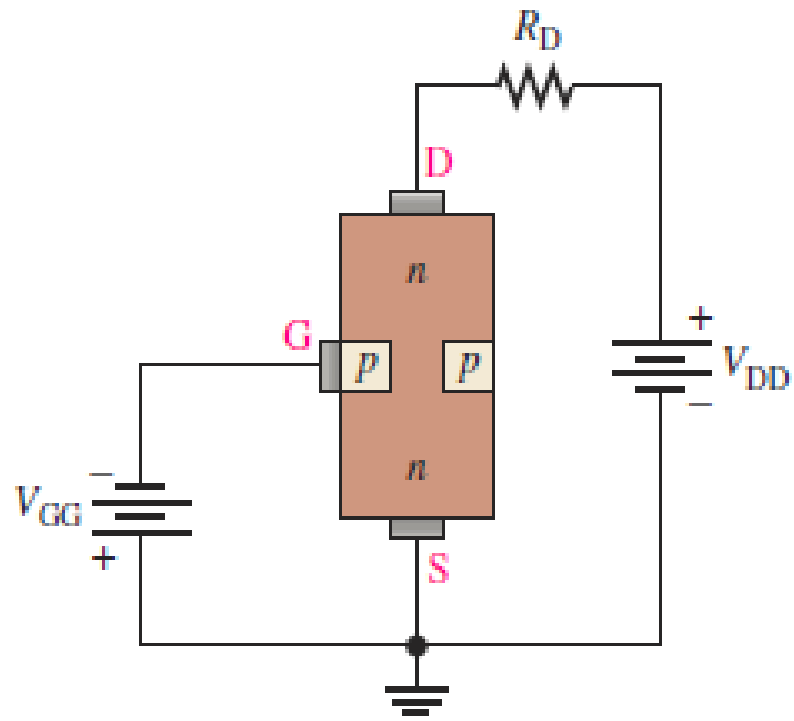
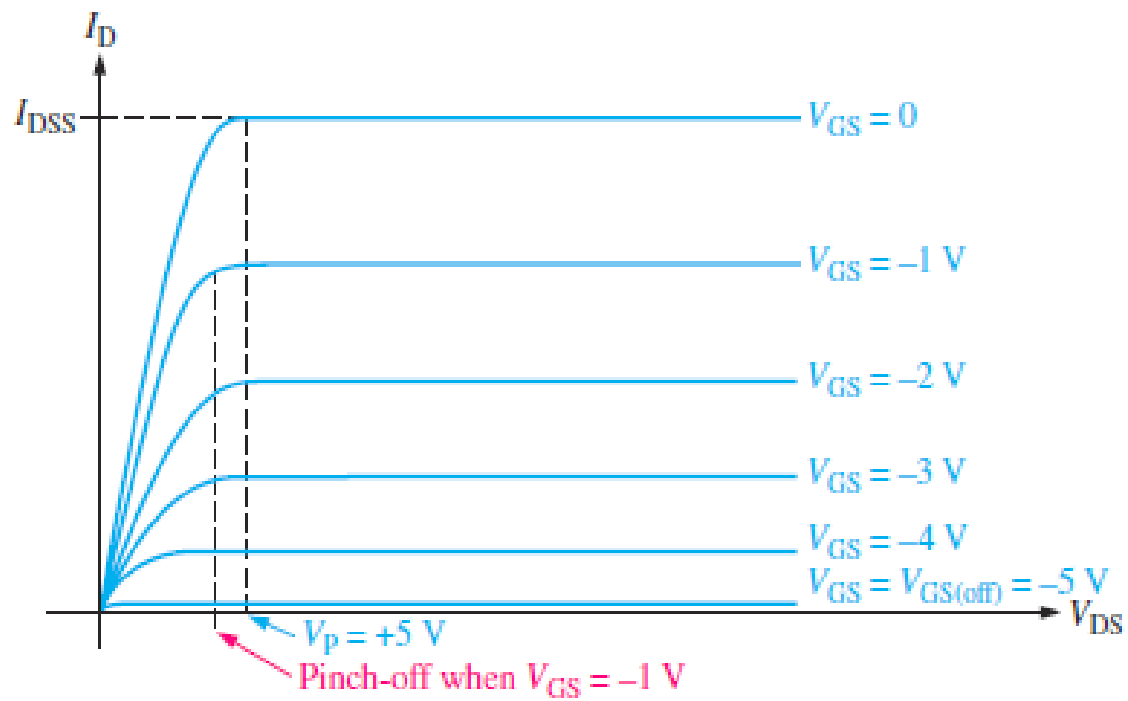


FET

Biassing

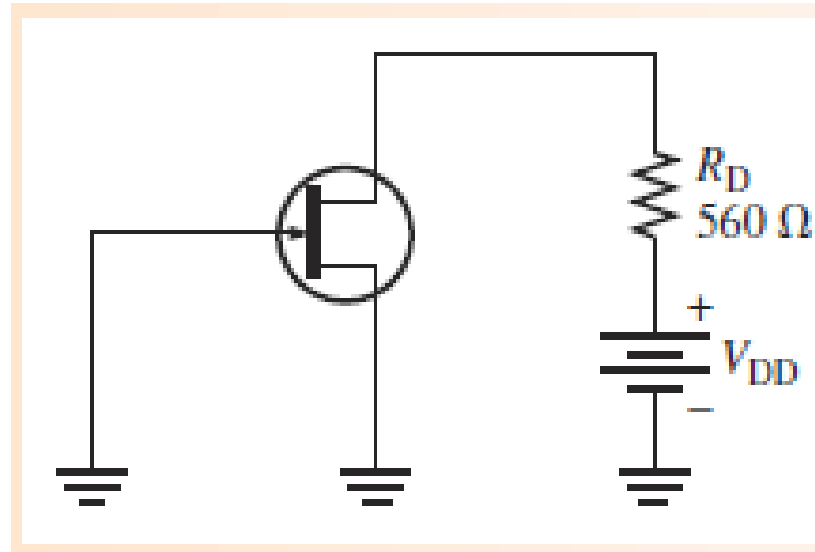






(b) Family of drain characteristic curves

$$V_{GS(\text{off})} = -4 \text{ V and } I_{DSS} = 12 \text{ mA.}$$



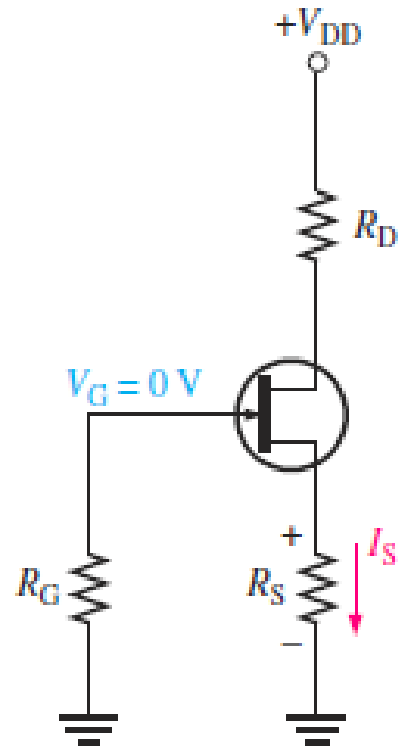
minimum value of V_{DD} required to put the device in the constant-current region of operation when $V_{GS} = 0 \text{ V}$.

$$V_{DS} = V_P = 4 \text{ V}$$

$$V_{DD} = V_{DS} + V_{R_D} = 4 \text{ V} + 6.72 \text{ V} = 10.7 \text{ V}$$

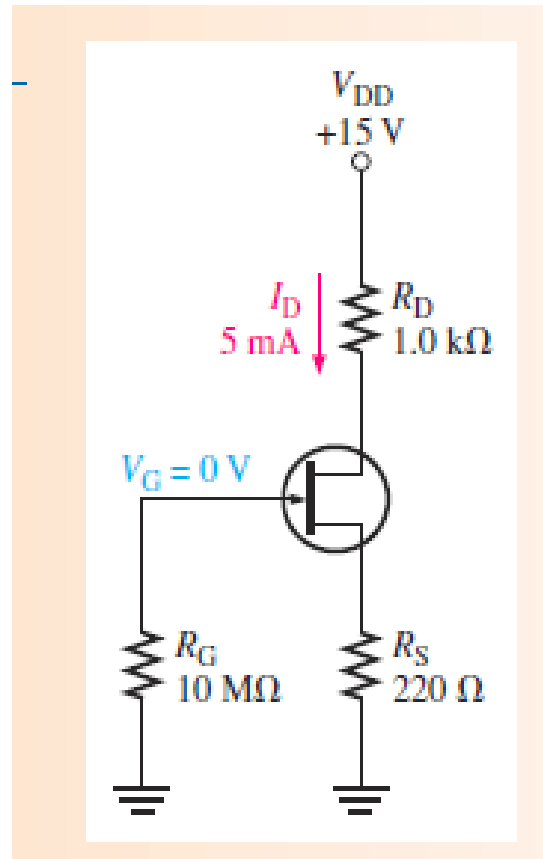
$$V_{R_D} = I_D R_D = (12 \text{ mA})(560 \Omega) = 6.72 \text{ V}$$

Self bias



(a) n channel

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$



$$V_S = I_D R_S = (5 \text{ mA})(220 \Omega) = 1.1 \text{ V}$$

$$V_D = V_{DD} - I_D R_D = 15 \text{ V} - (5 \text{ mA})(1.0 \text{ k}\Omega) = 15 \text{ V} - 5 \text{ V} = 10 \text{ V}$$

Therefore,

$$V_{DS} = V_D - V_S = 10 \text{ V} - 1.1 \text{ V} = 8.9 \text{ V}$$

Since $V_G = 0 \text{ V}$,

$$V_{GS} = V_G - V_S = 0 \text{ V} - 1.1 \text{ V} = -1.1 \text{ V}$$

(10V,
5mA)

Ayan Biswas

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Sagnik Das

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Sarit Roy Chaudhury

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Asipi Praveen Rao

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Arup Baral

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Abhishek Sarkar

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Mayukhmali Das

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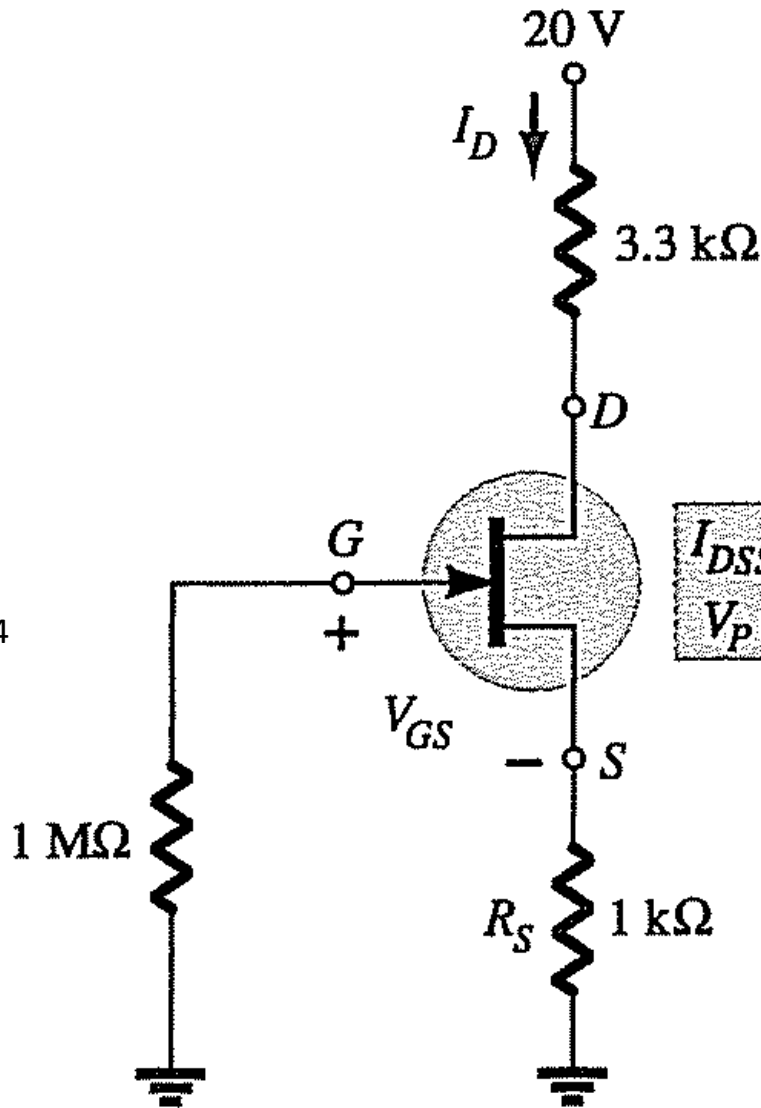
Mayukhmali Das 001910701098

Chayan Talukder

$$V_{DS} = 20 - 4.3 * 4 \\ = 2.8 \text{ V}$$

$$V_D = 6.8 \text{ V}$$

$$\text{For } I_D = 2 \text{ mA} \\ V_{DS} = 20 - 2 * 4.3 = 11.4$$



- V_{GSQ}
- I_{DQ}
- V_{DS}
- V_S
- V_G
- V_D

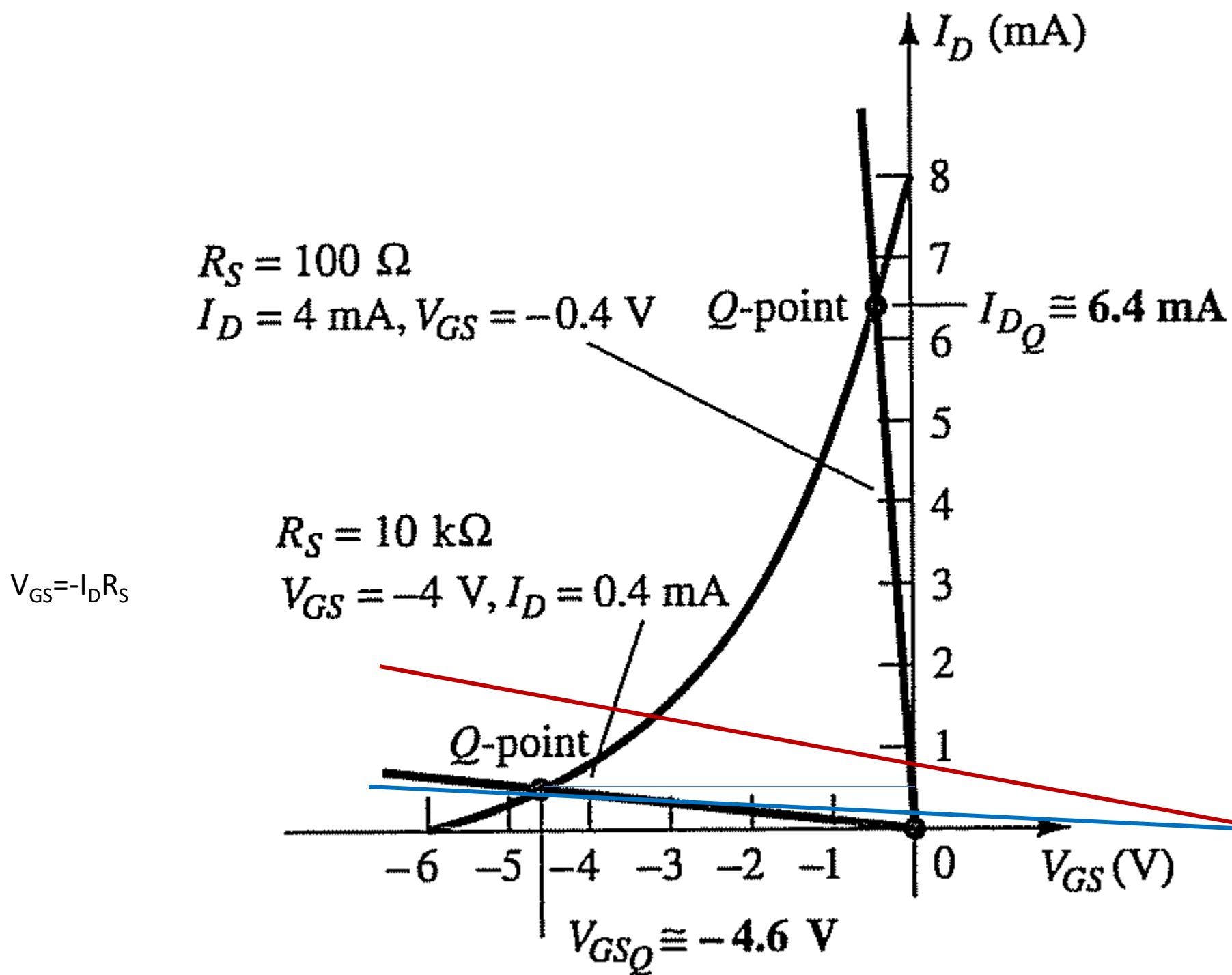
$$; I_D = 4 \text{ mA},$$

$$V_S = I_D R_S = 4V$$

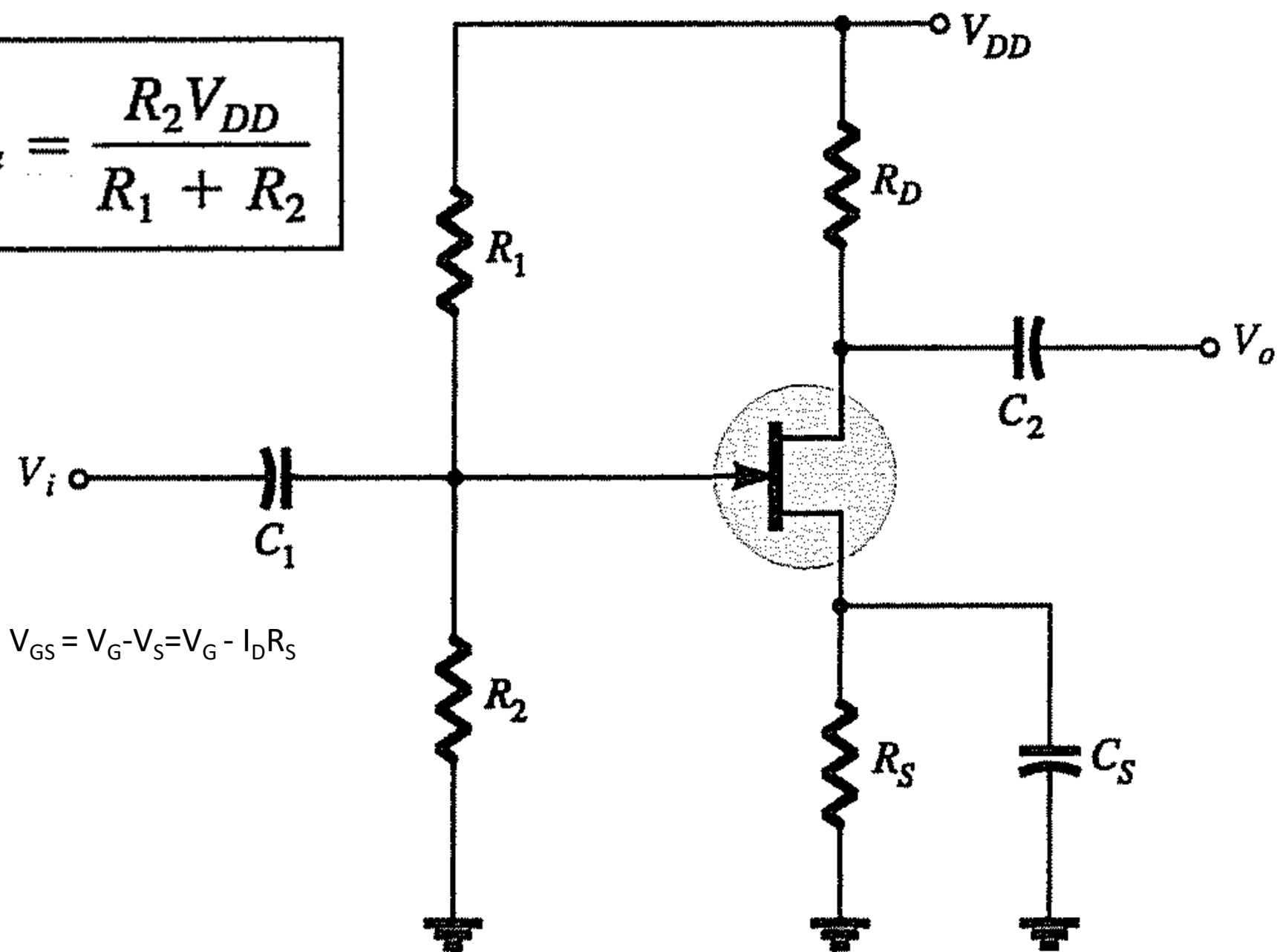
$$V_{GS} = V_G - V_S = -V_S$$

$$V_{GS} = -(4 \text{ mA})(1 \text{ k}\Omega) = -4 \text{ V}$$

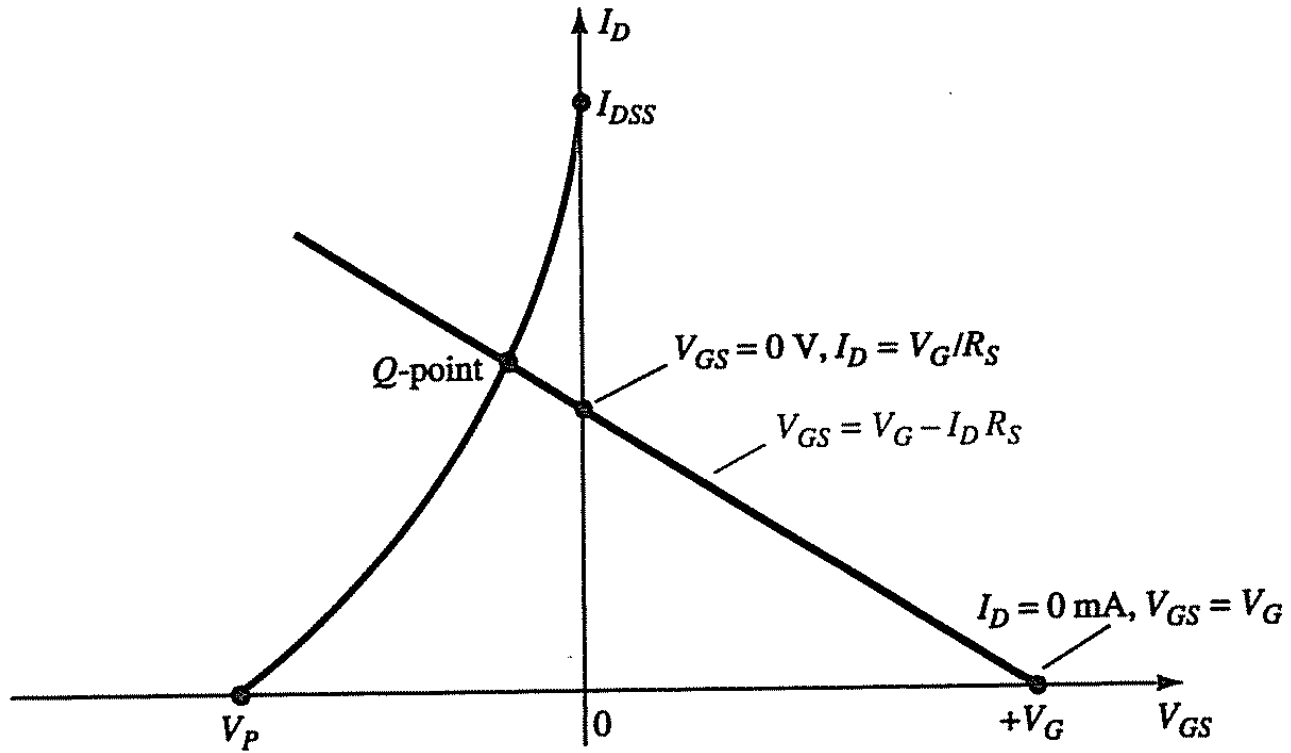
$$V_{DS} = 2.8 \text{ V}$$

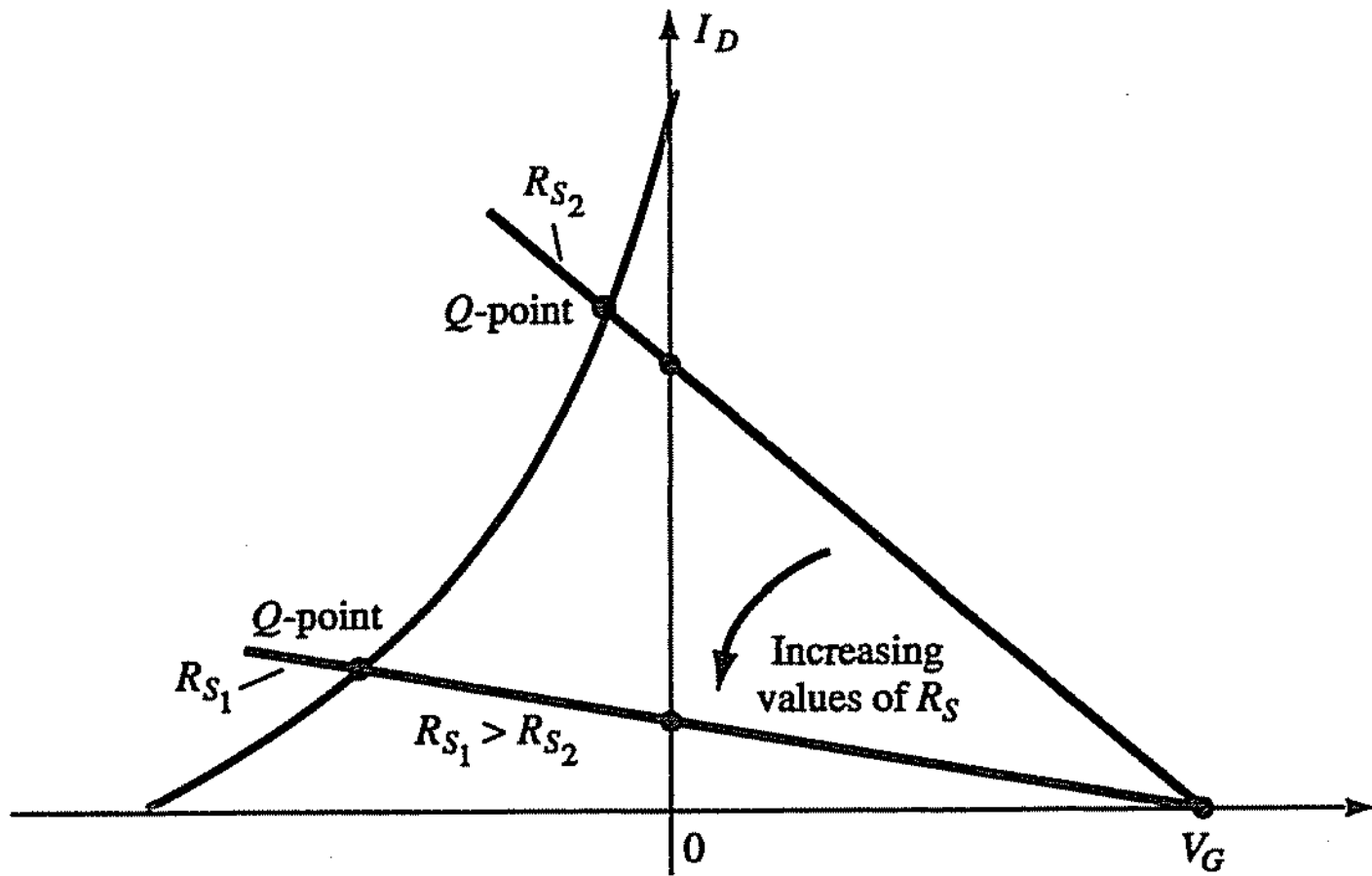


$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

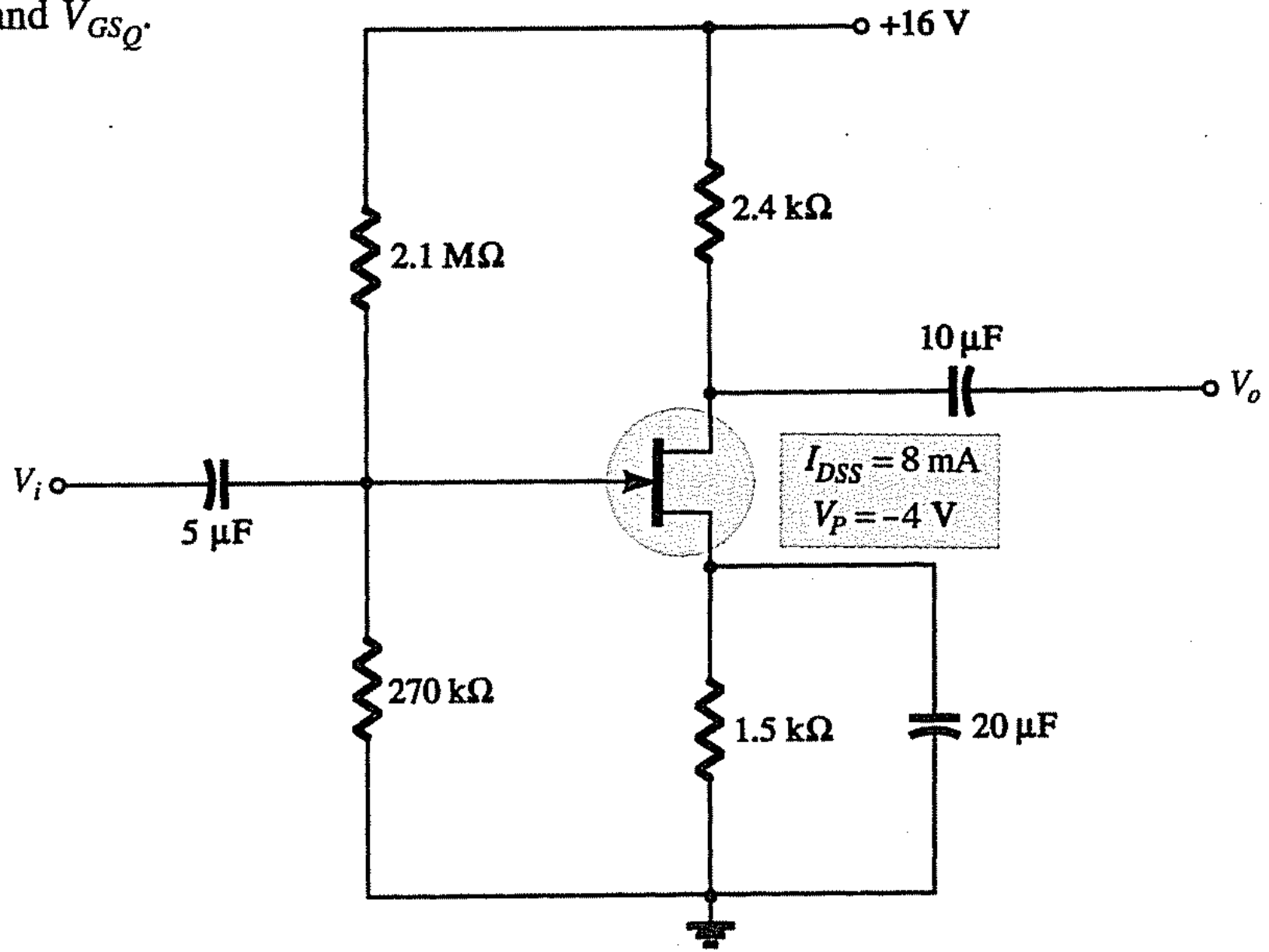


$$V_{GS} = V_G - V_S = V_G - I_D R_S$$





- a. I_{DQ} and V_{GSQ} .
- b. V_D .
- c. V_S .
- d. V_{DS} .
- e. V_{DG} .



$$\begin{aligned}V_G &= \frac{R_2 V_{DD}}{R_1 + R_2} \\&= \frac{(270 \text{ k}\Omega)(16 \text{ V})}{2.1 \text{ M}\Omega + 0.27 \text{ M}\Omega} \\&= 1.82 \text{ V}\end{aligned}$$

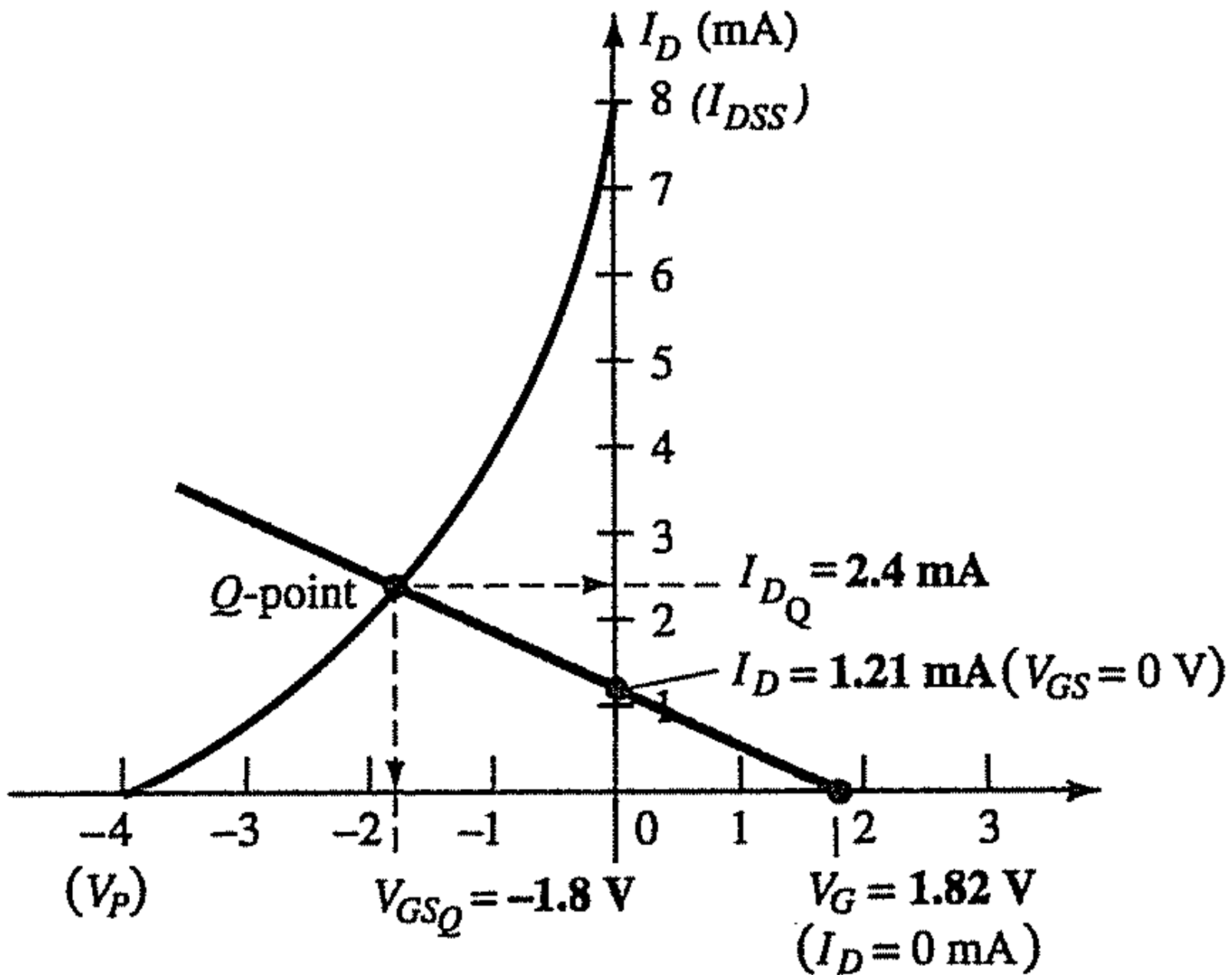
$$\begin{aligned}V_{GS} &= V_G - I_D R_S \\&= 1.82 \text{ V} - I_D (1.5 \text{ k}\Omega)\end{aligned}$$

When $I_D = 0 \text{ mA}$,

$$V_{GS} = +1.82 \text{ V}$$

When $V_{GS} = 0 \text{ V}$,

$$I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$



$$\begin{aligned} \text{b. } V_D &= V_{DD} - I_D R_D \\ &= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega) \\ &= \mathbf{10.24 \text{ V}} \end{aligned}$$

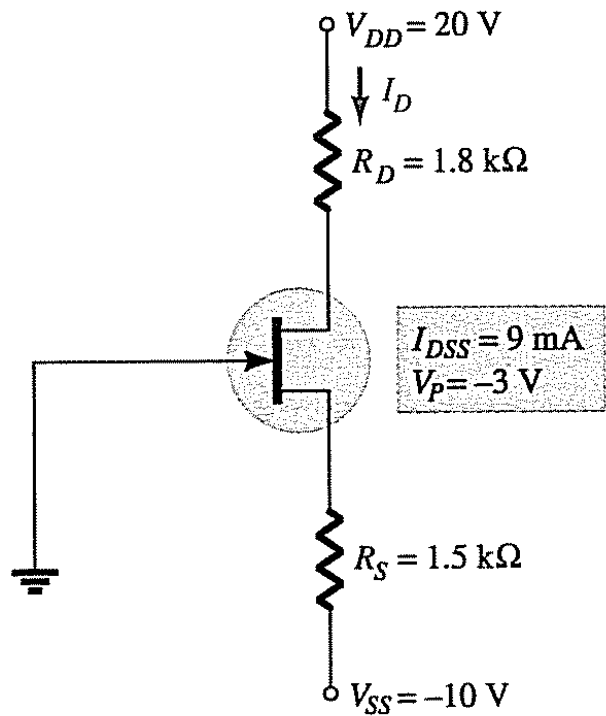
$$\begin{aligned} \text{c. } V_S &= I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega) \\ &= \mathbf{3.6 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{d. } V_{DS} &= V_{DD} - I_D (R_D + R_S) \\ &= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= \mathbf{6.64 \text{ V}} \end{aligned}$$

$$\begin{aligned} \text{or } V_{DS} &= V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V} \\ &= \mathbf{6.64 \text{ V}} \end{aligned}$$

$$\begin{aligned}V_{DG} &= V_D - V_G \\ &= 10.24 \text{ V} - 1.82 \text{ V} \\ &= \mathbf{8.42 \text{ V}}\end{aligned}$$

- a. I_{DQ} and V_{GSQ} .
- b. V_{DS} .
- c. V_D .
- d. V_S .



DEPLETION-TYPE MOSFETs

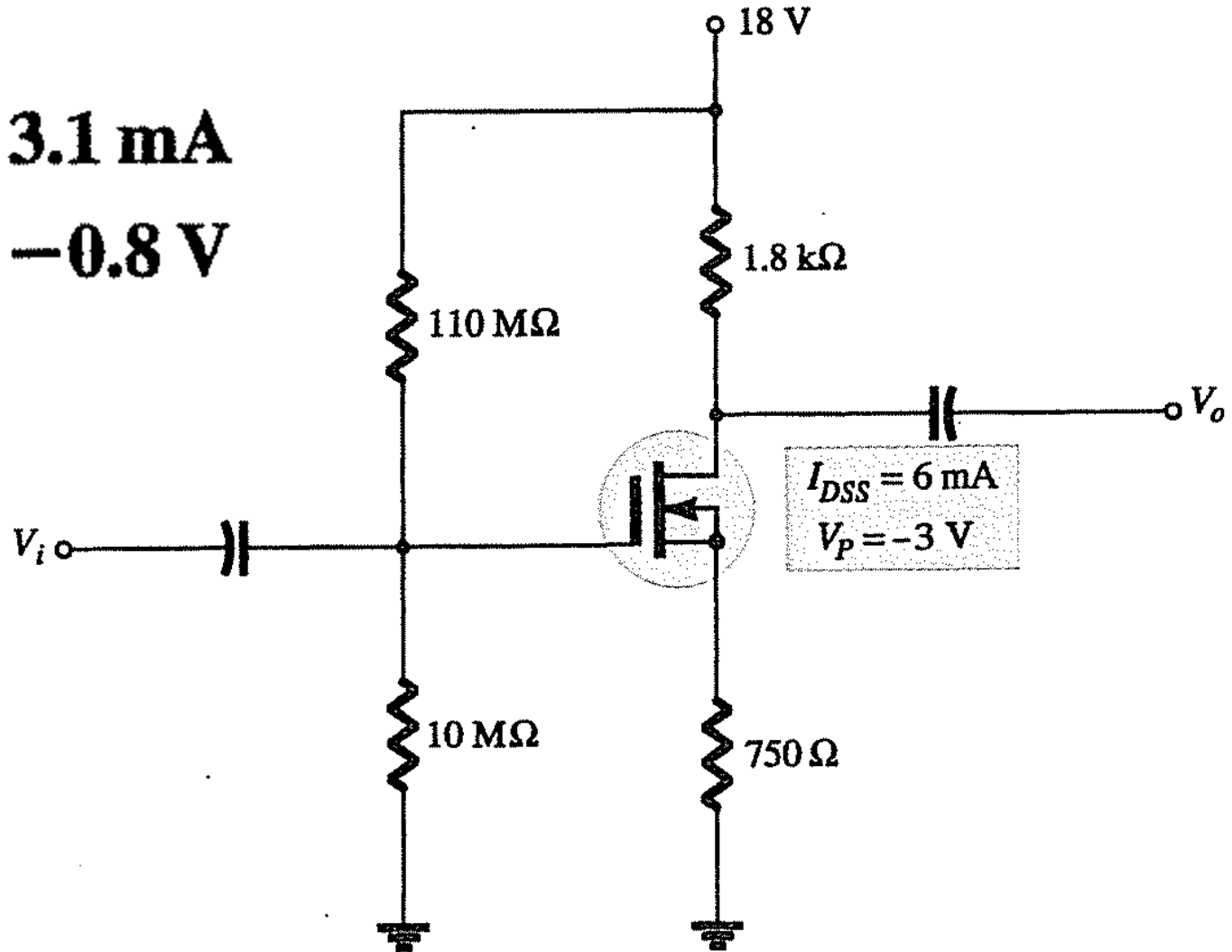
Normally ON

- a. I_{DQ} and V_{GSQ}
 b. V_{DS}

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

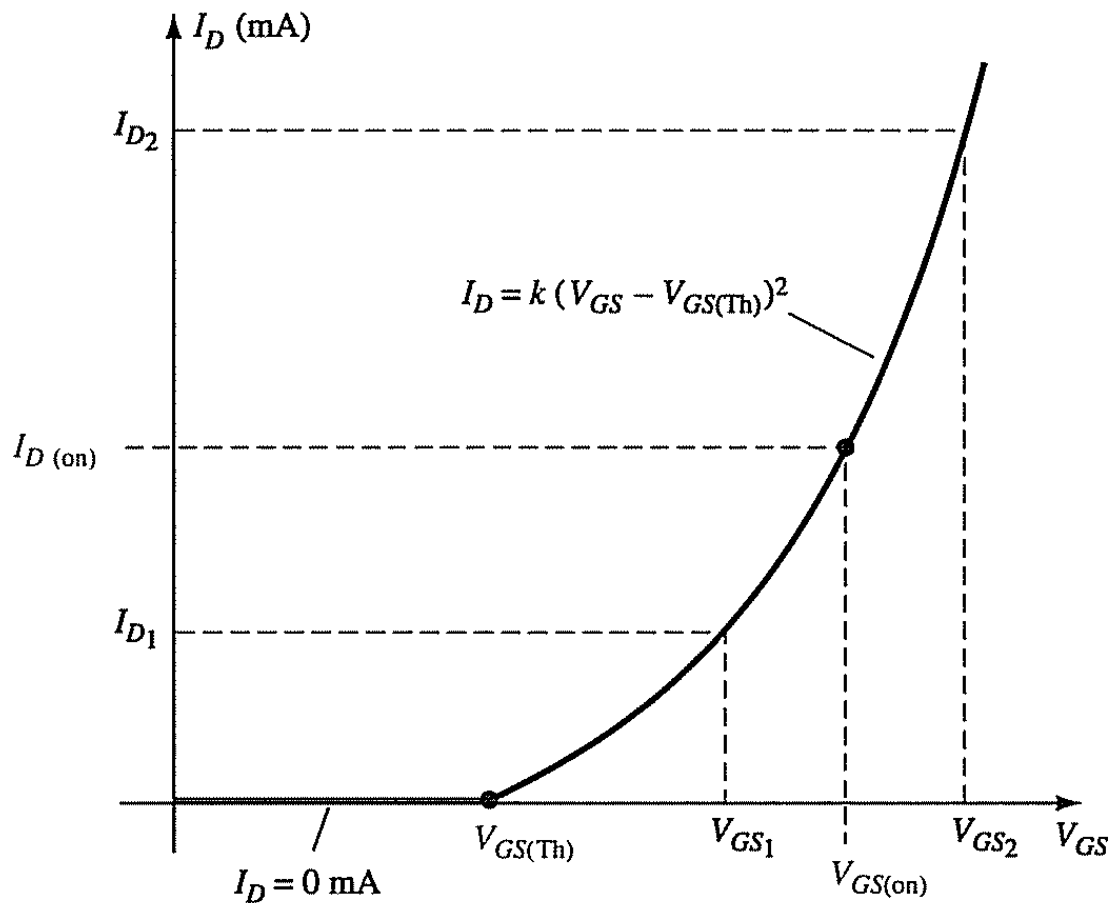
$$I_{DQ} = 3.1 \text{ mA}$$

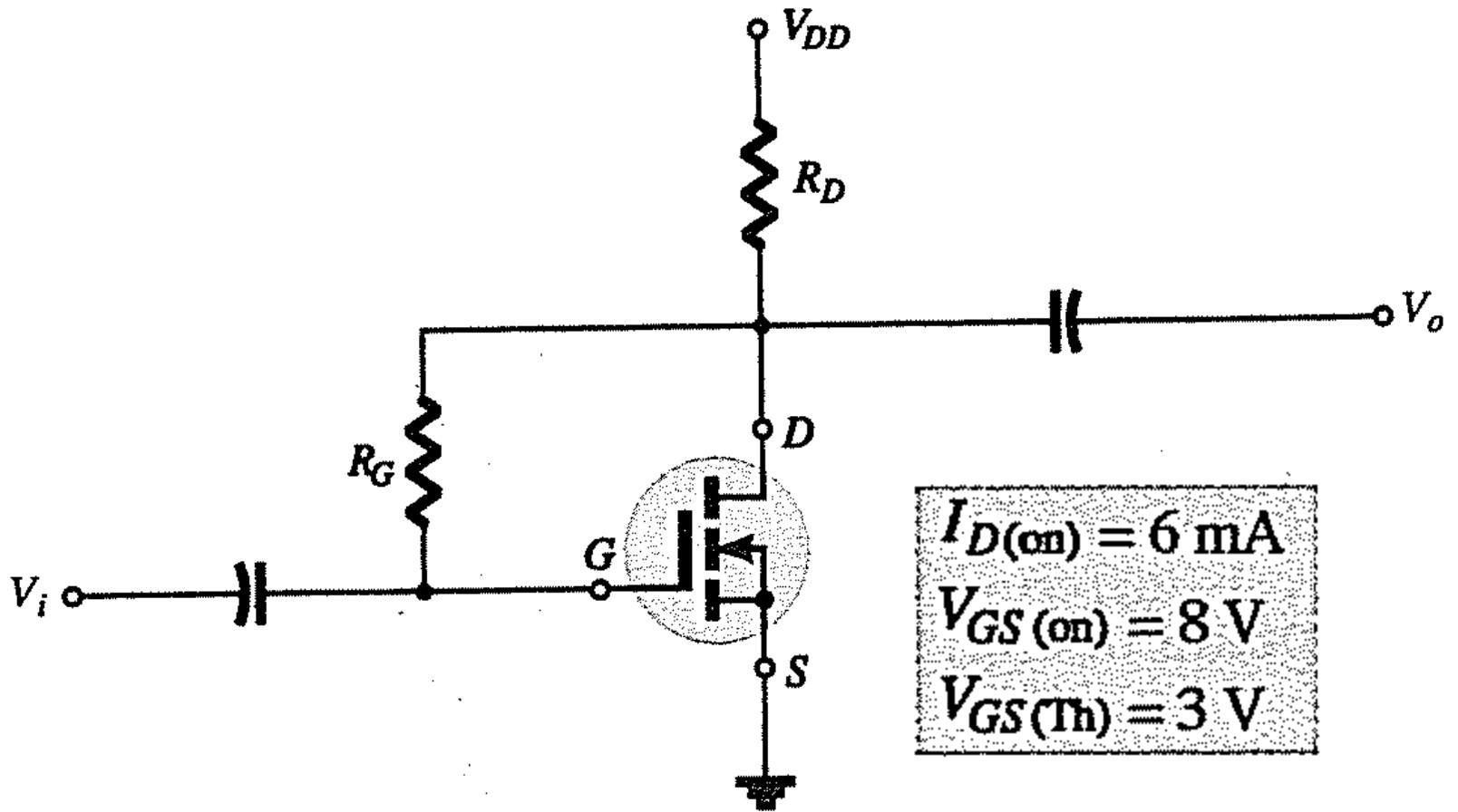
$$V_{GSQ} = -0.8 \text{ V}$$



ENHANCEMENT-TYPE MOSFETS

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$





$R_D = 2 \text{ k}$
 $R_G = 10 \text{ M}$
 $V_{DD} = 12 \text{ V}$

$$\begin{aligned}
 k &= \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \\
 &= \frac{6 \text{ mA}}{(8 \text{ V} - 3 \text{ V})^2} = \frac{6 \times 10^{-3}}{25} \text{ A/V}^2 \\
 &= 0.24 \times 10^{-3} \text{ A/V}^2
 \end{aligned}$$

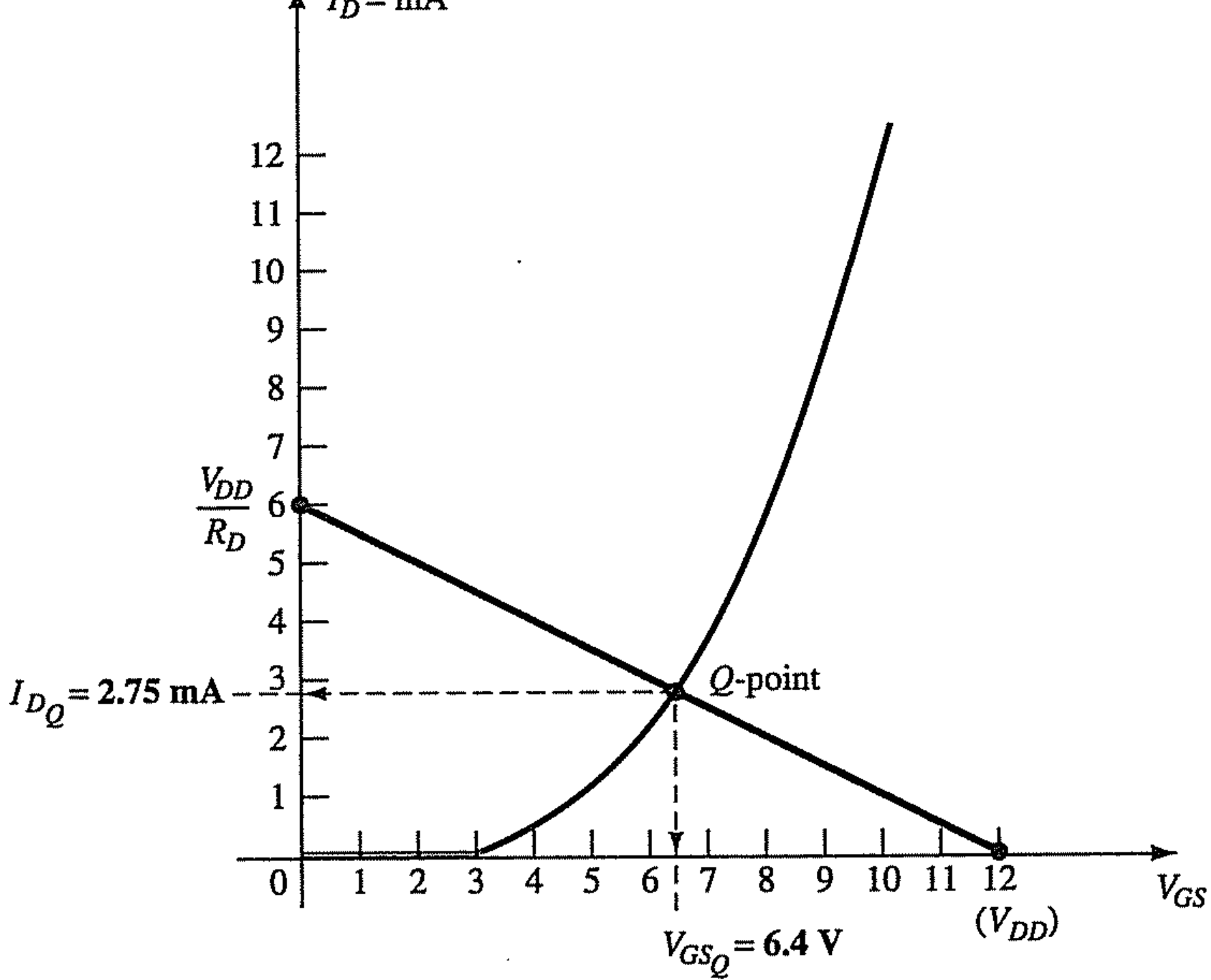
$$I_D = 0.24 \times 10^{-3} (6 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3} (9) \\ = 2.16 \text{ mA}$$

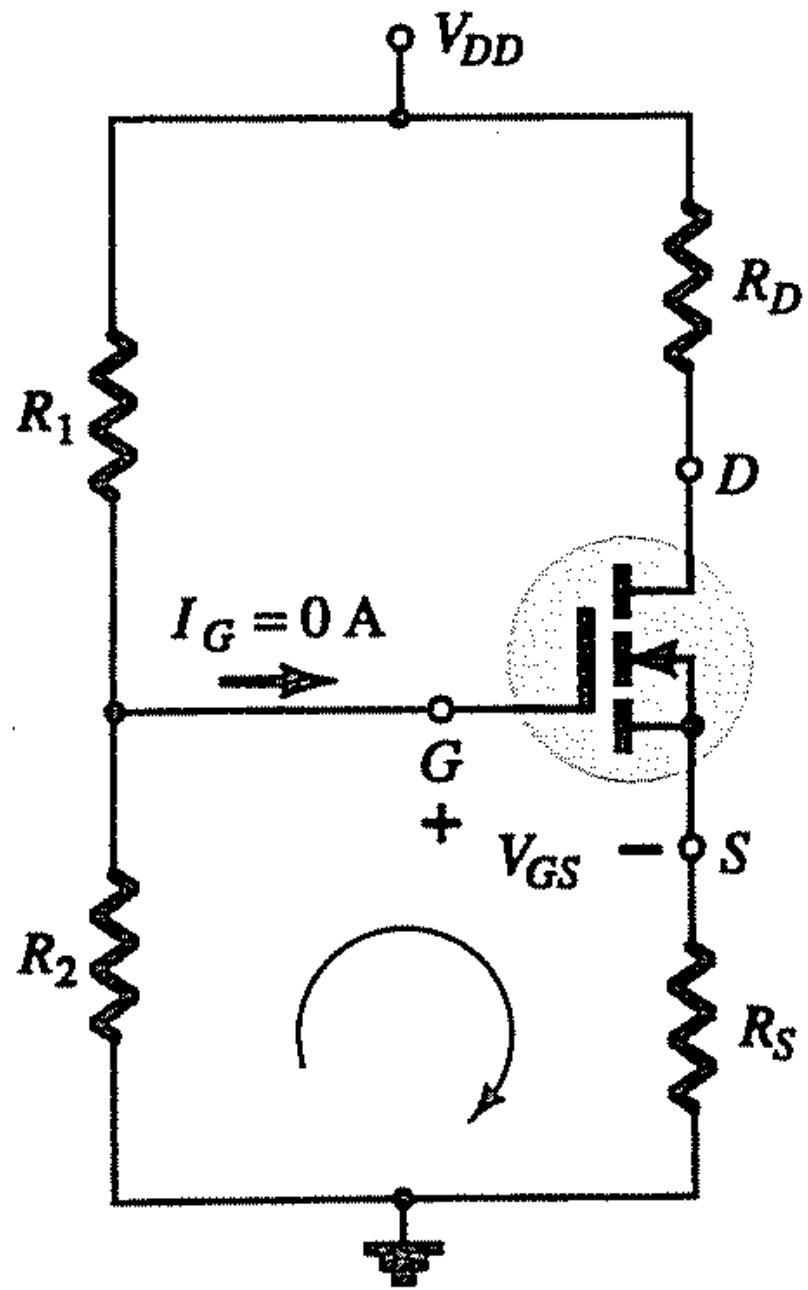
$$I_D = 0.24 \times 10^{-3} (10 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3} (49) \\ = 11.76 \text{ mA}$$

$$V_{GS} = V_{DD} - I_D R_D \\ = 12 \text{ V} - I_D (2 \text{ k}\Omega)$$

$$V_{GS} = V_{DD} = 12 \text{ V} \Big|_{I_D=0 \text{ mA}}$$

$$I_D = \frac{V_{DD}}{R_D} = \frac{12 \text{ V}}{2 \text{ k}\Omega} = 6 \text{ mA} \Big|_{V_{GS}=0 \text{ V}}$$





$$V_{GS} = V_G - I_D R_S$$

	075
	090
	015
	012
Avirup	100
	017
	098
	016
	042
	022
	027
	013
	096
	014
	067
	011
	076
	010
	057
	019
	093
	068
	024
	074
	040
	03
	052
	008
	020
	041
	078
	073
	101
	006
	045
	083
	030

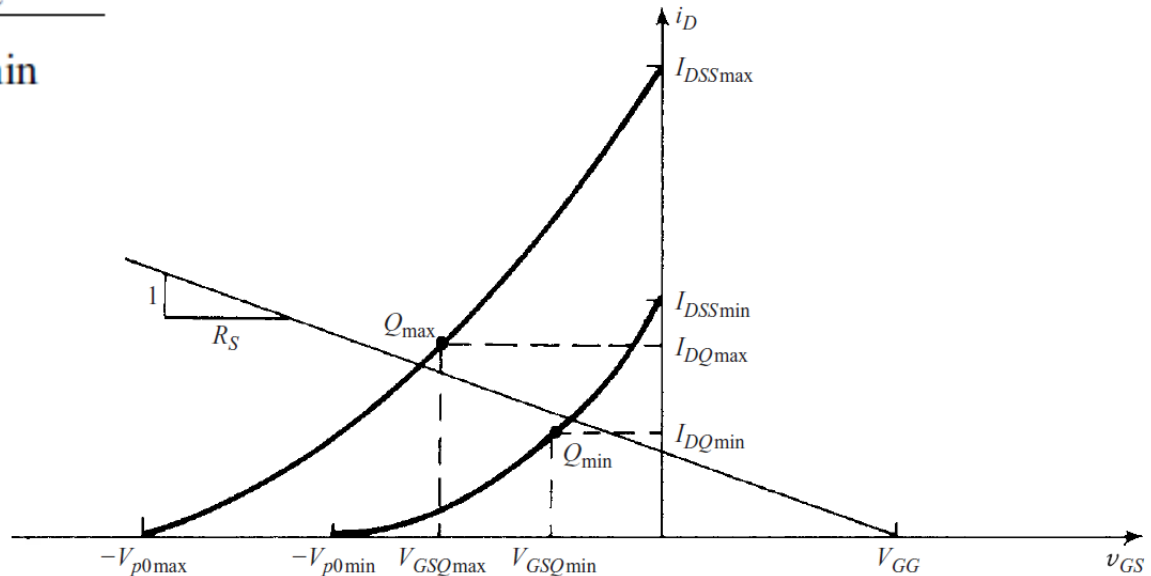
Just as β may vary in the BJT, the JFET shorted-gate parameters I_{DSS} and V_{p0} can vary widely within devices of the same classification. It is, however, possible to set the gate-source bias so that, in spite of this variation, the Q point (and hence the quiescent drain current) is confined within fixed limits.

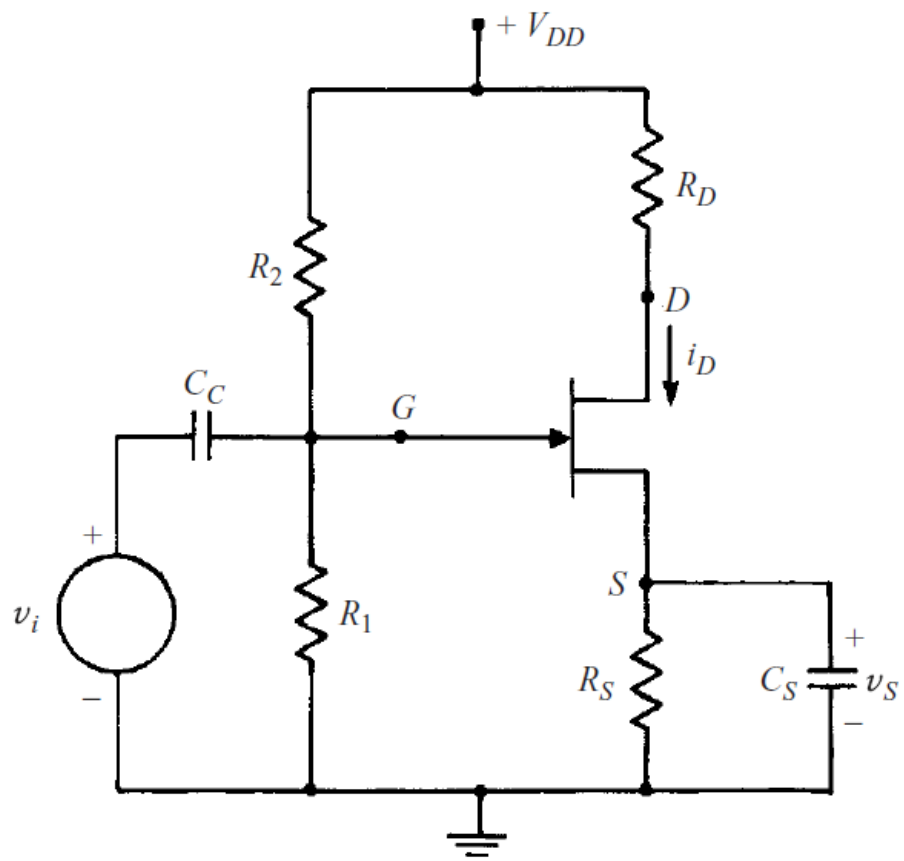
The extremes of FET parameter variation are usually specified by the manufacturer, and may be used to establish upper and lower (worst-case) transfer characteristics. The upper and lower quiescent points Q_{max} and Q_{min} are determined by their ordinates I_{DQmax} and I_{DQmin} ; we assign I_{DQmax} and I_{DQmin} as the limits of allowable variation of I_{DQ} along a dc load line superimposed on the family of nominal drain characteristics. (These in turn establish V_{DSQmax} and V_{DSQmin} , respectively.)

This dc load line is established by choosing R_D & R_S in a circuit like that of Fig. 4-5 so that v_{DS} remains within a desired region of the nominal drain characteristics.

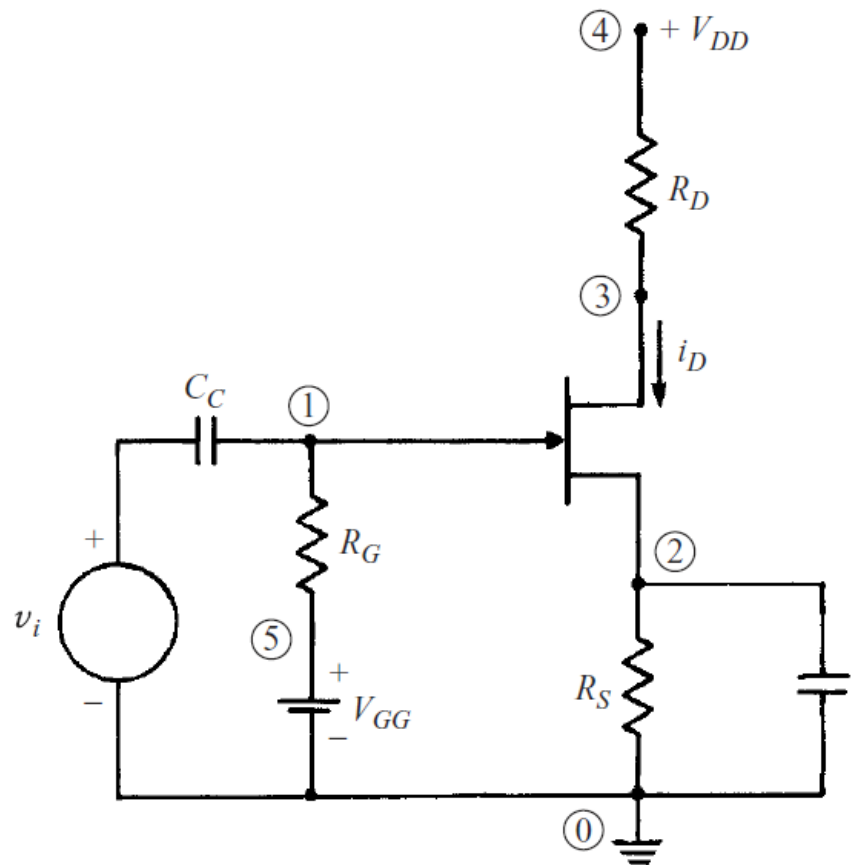
If now a value of R_S is selected such that

$$R_S \geq \frac{|V_{GSQmax} - V_{GSQmin}|}{I_{DQmax} - I_{DQmin}}$$





(a)



(b)

Fig. 4-5

Then the transfer bias line with slope $1/R_S$ and v_{GS} intercept $V_{GG} - 0$ is located as shown in Fig. 5-3, and the nominal Q point is forced to lie beneath Q_{max} and above Q_{min} , so that, as desired, $I_{DQmin} < I_{DQ} < I_{DQmax}$. With $R_S; R_D$, and V_{GG} already assigned, R_G is chosen large enough to give a satisfactory input impedance, and then R_1 and R_2 are determined from (4.3). Generally, R_S will be comparable in magnitude to R_D . To obtain desirable ac gains, a bypass capacitor must be used with R_S , and an ac load line introduced; they are analyzed with techniques similar to those of Section 3.

5.26 The self-biased JFET of Fig. 4-19 has a set of worst-case shorted-gate parameters that yield the plots of Fig. 5-15. Let $V_{DD} = 24\text{ V}$, $R_D = 3\text{ k}\Omega$, $R_S = 1\text{ k}\Omega$, and $R_G = 10\text{ M}\Omega$. (a) Find the range of I_{DQ} that can be expected. (b) Find the range of V_{DSQ} that can be expected. (c) Discuss the idea of reducing I_{DQ} variation by increasing the value of R_S .

(a) Since $V_{GG} = 0$, the transfer bias line must pass through the origin of the transfer characteristics plot, and its slope is $-1/R_S$ (solid line in Fig. 5-15). From the intersections of the transfer bias line and the transfer characteristics, we see that $I_{DQ\text{max}} \approx 2.5\text{ mA}$ and $I_{DQ\text{min}} \approx 1.2\text{ mA}$.

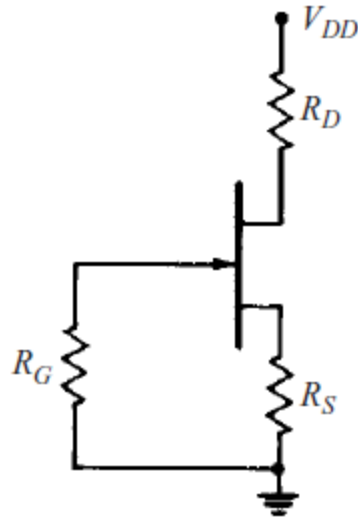


Fig. 4-19

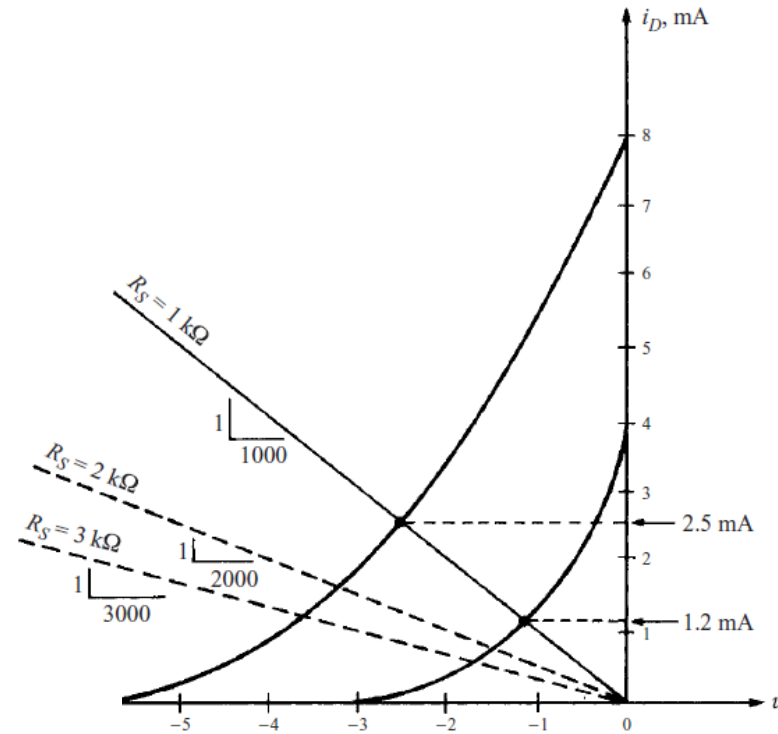


Fig. 5-15

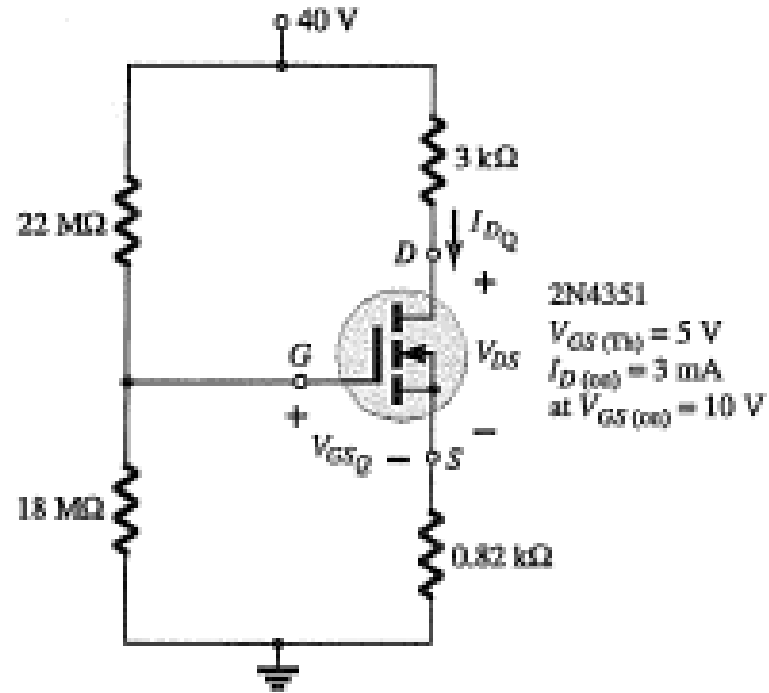
(b) For $I_{DQ} = I_{DQ\text{max}}$, KVL requires that

$$V_{DSQ\text{max}} = V_{DD} - I_{DQ\text{max}}(R_S + R_D) = 24 - (2.5)(1 + 3) = 14\text{ V}$$

And, for $I_{DQ\text{min}}$,

$$V_{DSQ\text{min}} = V_{DD} - I_{DQ\text{min}}(R_S + R_D) = 24 - (1.2)(1 + 3) = 19.2\text{ V}$$

(c) The transfer bias lines for $R_S = 2\text{ k}\Omega$ and $3\text{ k}\Omega$ are also plotted on Fig. 5-15 (dashed lines). An increase in R_S obviously does decrease the difference between $I_{DQ\text{max}}$ and $I_{DQ\text{min}}$; however, in the process I_{DQ} is reduced to quite low values, so that operation is on the nonlinear portion of the drain characteristics near the ohmic region where appreciable signal distortion results. But if self-bias with an external source is utilized (see Problems 5.27 and 5.48), the transfer bias line can be given a small negative slope without forcing I_{DQ} to approach zero.



$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18 \text{ M}\Omega)(40 \text{ V})}{22 \text{ M}\Omega + 18 \text{ M}\Omega} = 18 \text{ V}$$

$$V_{GS} = V_G - I_D R_S = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

Draw load line

When $I_D = 0 \text{ mA}$,

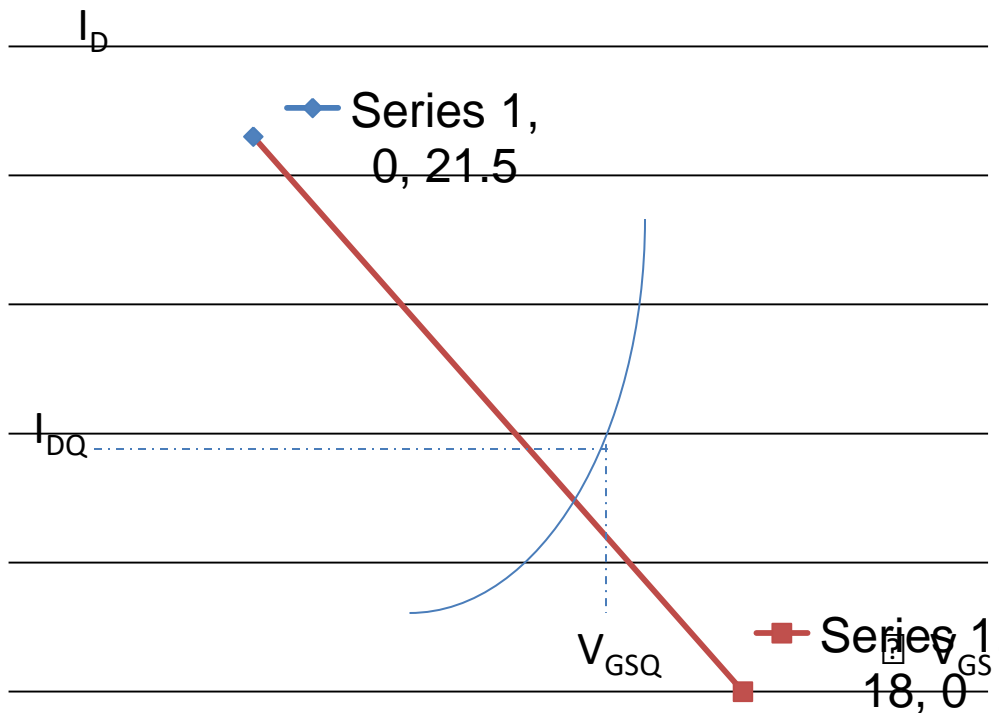
$$V_{GS} = 18 \text{ V} - (0 \text{ mA})(0.82 \text{ k}\Omega) = 18 \text{ V}$$

as appearing on Fig. 7.45. When $V_{GS} = 0 \text{ V}$,

$$V_{GS} = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

$$0 = 18 \text{ V} - I_D(0.82 \text{ k}\Omega)$$

$$I_D = \frac{18 \text{ V}}{0.82 \text{ k}\Omega} = 21.95 \text{ mA}$$



$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$

$$= \frac{3 \text{ mA}}{(10 \text{ V} - 5 \text{ V})^2} = 0.12 \times 10^{-3} \text{ A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(th)})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

$$I_{DQ} \cong 6.7 \text{ mA}$$

$$V_{GSQ} = 12.5 \text{ V}$$

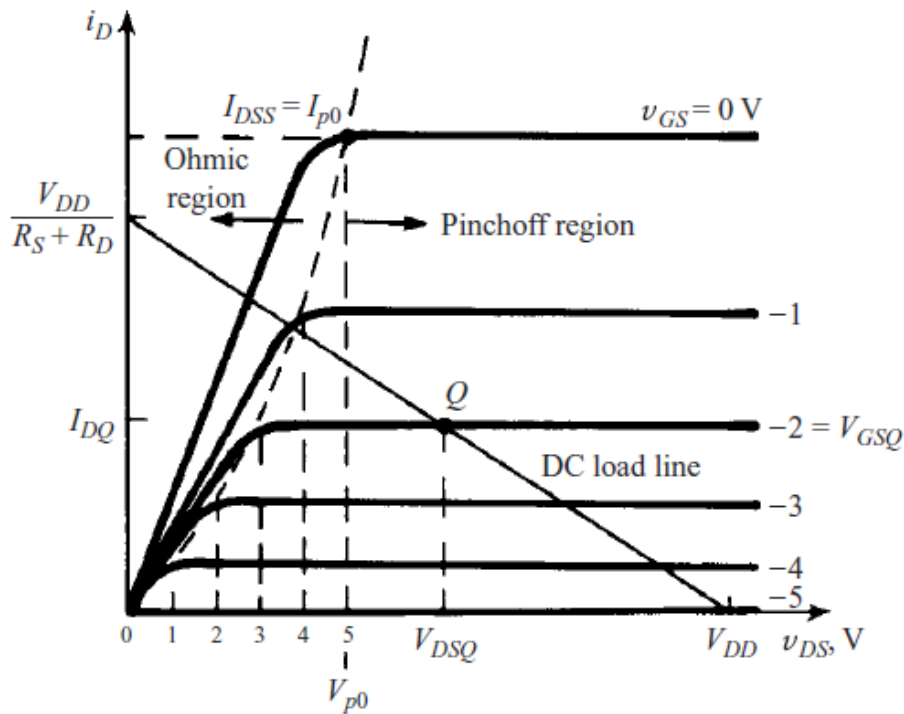
$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40 \text{ V} - (6.7 \text{ mA})(0.82 \text{ k}\Omega + 3.0 \text{ k}\Omega)$$

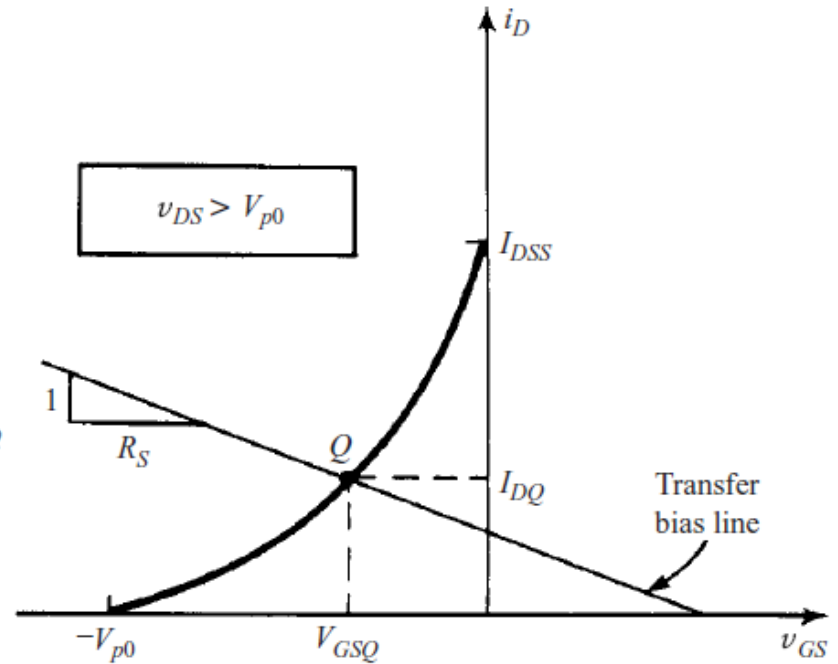
$$= 40 \text{ V} - 25.6 \text{ V}$$

$$= 14.4 \text{ V}$$

SMALL-SIGNAL EQUIVALENT CIRCUITS FOR THE FET



(a) Drain characteristics



(b) Transfer characteristic

Variable

Meaning

i_D, v_{GS}

Total instantaneous values

I_D, V_{GS}

DC values

i_d, v_{gs}

Instantaneous ac values

I_d, V_{gs}

Phasor values

$$i_D = f(v_{GS}, v_{DS})$$

$$v_{GS} = V_{GSQ} + v_i = V_{GSQ} + v_{gs}$$

$$i_D = K_n(v_{GS} - V_{TN})^2$$

$$i_D = K_n[V_{GSQ} + v_{gs} - V_{TN}]^2 = K_n[(V_{GSQ} - V_{TN}) + v_{gs}]^2$$

or

$$i_D = K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs} + K_nv_{gs}^2$$

$$v_{gs} \ll 2(V_{GSQ} - V_{TN})$$

$$i_D = I_D + i_d$$

$$i_d = 2K_n(V_{GSQ} - V_{TN})v_{gs}$$

$$g_m = \frac{i_d}{v_{gs}} = 2K_n(V_{GSQ} - V_{TN})$$

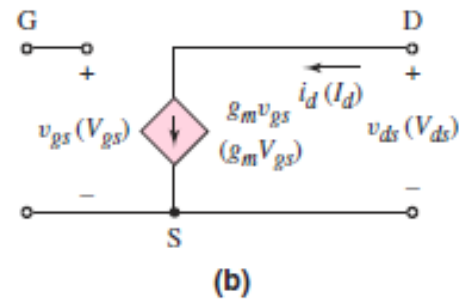
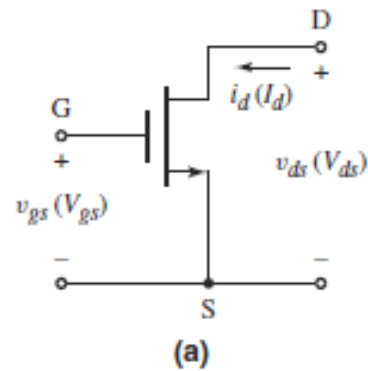
$$g_m = 2\sqrt{K_n I_{DQ}}$$

Consider an n-channel MOSFET with parameters $V_{TN} = 0.4 \text{ V}$, $k'_n = 100 \mu\text{A}/\text{V}^2$, and $W/L = 25$. Assume the drain current is $I_D = 0.40 \text{ mA}$.

$$K_n = \frac{k'_n}{2} \cdot \frac{W}{L} = \left(\frac{0.1}{2}\right)(25) = 1.25 \text{ mA}/\text{V}^2$$

$$g_m = 2\sqrt{K_n I_D Q} = 2\sqrt{(1.25)(0.4)} = 1.41 \text{ mA}/\text{V}$$

mS



$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})]$$

$$r_{ds} = r_o = \left(\frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Big|_{v_{GS}=V_{GSQ}=\text{const.}}$$

$$r_o = [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1} \cong [\lambda I_{DQ}]^{-1}$$

$$i_d = \Delta i_D \approx di_D = g_m v_{gs} + \frac{1}{r_{ds}} v_{ds}$$

$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q \approx \left. \frac{\Delta i_D}{\Delta v_{GS}} \right|_Q \quad \square \text{ transconductance}$$

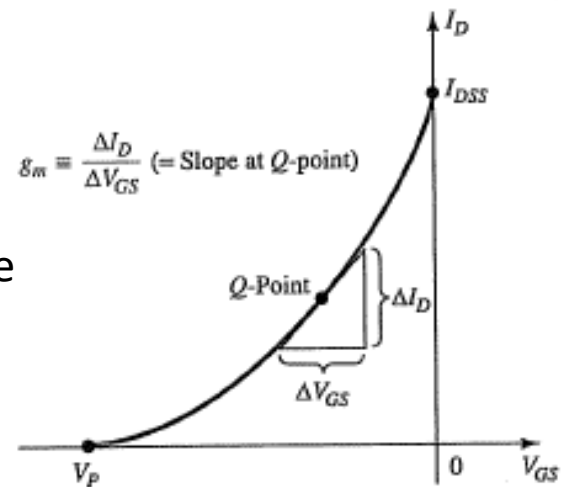
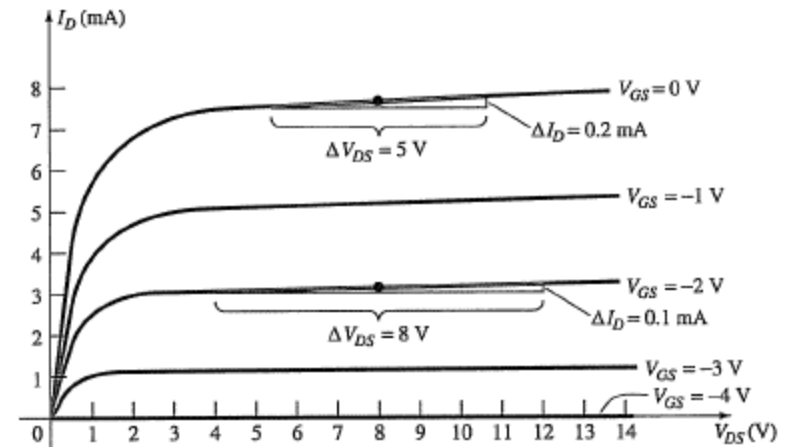
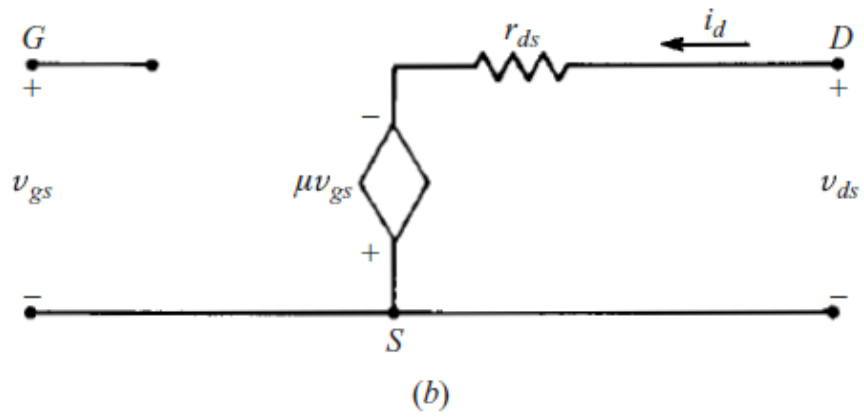
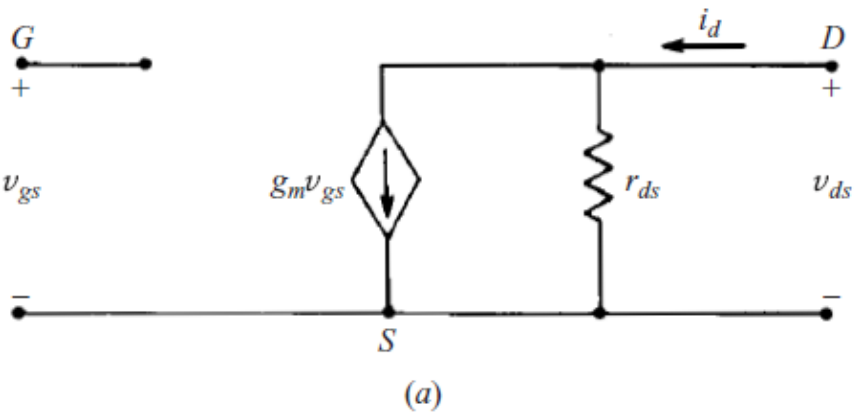


FIG. 8.1

$$r_{ds} \equiv \left. \frac{\partial v_{DS}}{\partial i_D} \right|_Q \approx \left. \frac{\Delta v_{DS}}{\Delta i_D} \right|_Q \quad \square \text{ Source to drain resistance}$$



AC Equivalent Circuit

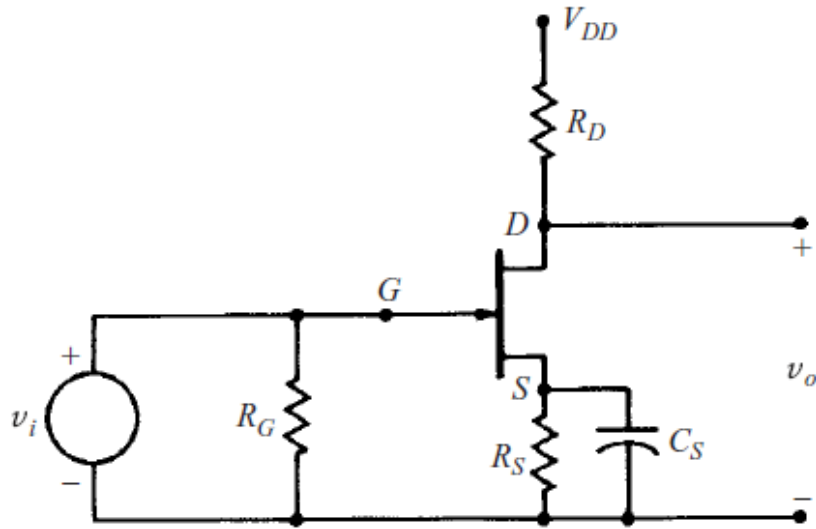


S

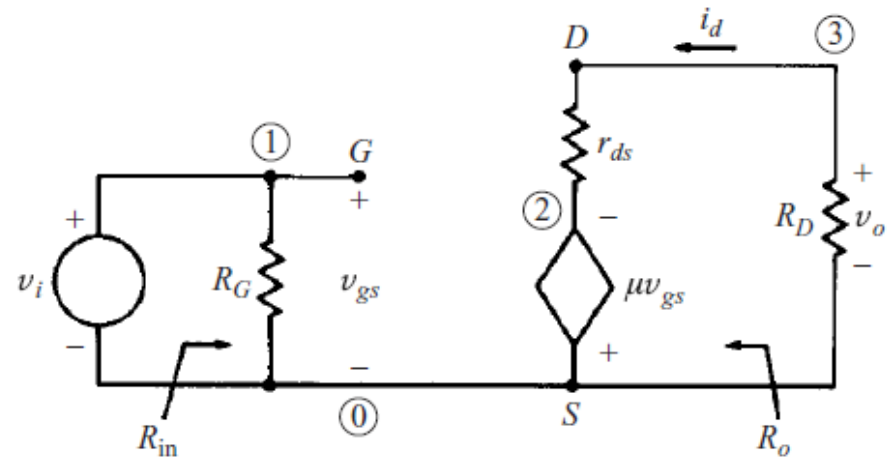
$\mu_D v_{gd}$

D

$$(\mu+1)v_{gs} = v_{gd}$$



(a) CS amplifier



(b) Small-signal equivalent circuit

$$v_o = -\frac{R_D}{R_D + r_{ds}} \mu v_{gs}$$

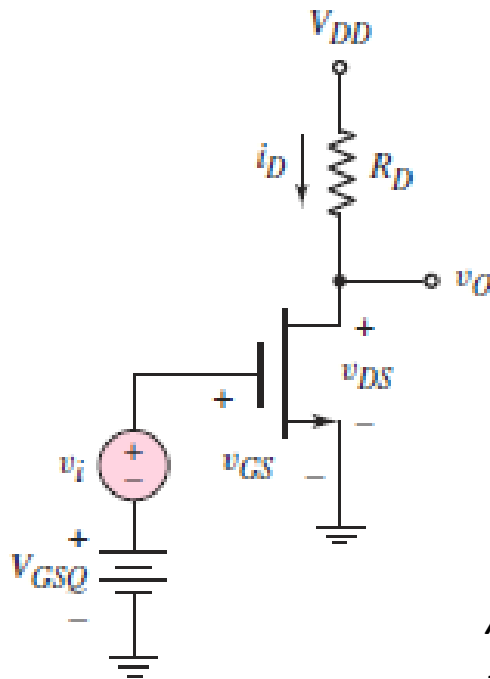
$$A_v = \frac{v_o}{v_i} = -\frac{\mu R_D}{R_D + r_{ds}} = -g_m r_{ds} \parallel R_D$$

let $R_D = 3 \text{ k}\Omega$, $\mu = 60$, and $r_{ds} = 30 \text{ k}\Omega$.

$$A_v = -\frac{(60)(3 \times 10^3)}{3 \times 10^3 + 30 \times 10^3} = -5.45$$

assume parameters are: $V_{GSQ} = 2.12 \text{ V}$, $V_{DD} = 5 \text{ V}$,
 and $R_D = 2.5 \text{ k}\Omega$. Assume transistor parameters are: $V_{TN} = 1 \text{ V}$, $K_n = 0.80$
 mA/V^2 , and $\lambda = 0.02 \text{ V}^{-1}$. Assume the transistor is biased in the saturation region.

Find out small signal voltage gain



$$I_{DQ} \cong K_n(V_{GSQ} - V_{TN})^2 = (0.8)(2.12 - 1)^2 = 1.0 \text{ mA}$$

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 5 - (1)(2.5) = 2.5 \text{ V}$$

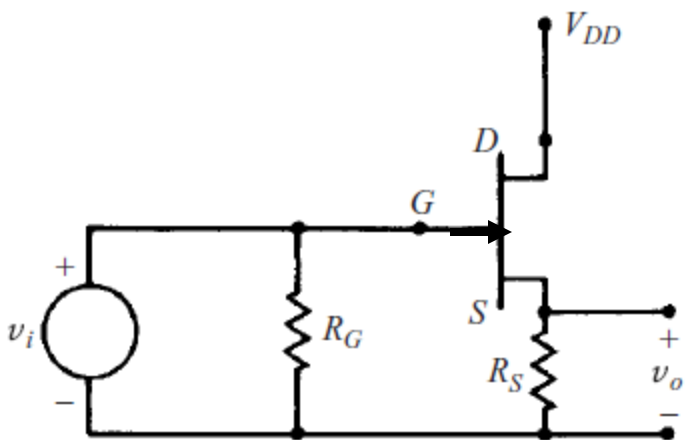
$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(0.8)(2.12 - 1) = 1.79 \text{ mA/V}$$

$$r_o = [\lambda I_{DQ}]^{-1} = [(0.02)(1)]^{-1} = 50 \text{ k}\Omega$$

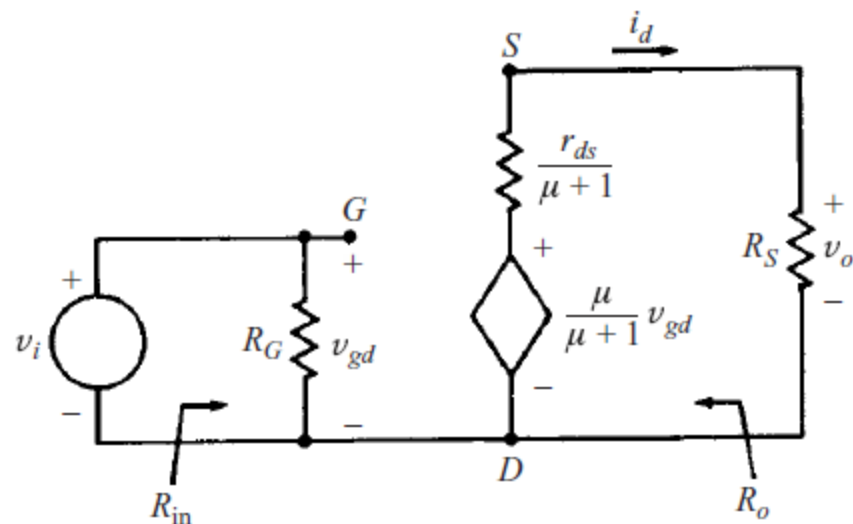
$$V_o = -g_m V_{gs}(r_o \parallel R_D)$$

$$-(1.79)(50 \parallel 2.5) = -4.26$$

$$A_v =$$



(a) CD or SF amplifier



(b) Small-signal equivalent circuit

$$v_o = \frac{R_S}{R_S + r_{ds}/(\mu + 1)} \frac{\mu}{\mu + 1} v_{gd} = \frac{\mu R_S v_{gd}}{(\mu + 1)R_S + r_{ds}}$$

$$A_v = \frac{v_o}{v_i} = \frac{\mu R_S}{(\mu + 1)R_S + r_{ds}}$$

let $R_S = 5\text{ k}\Omega$, $\mu = 60$, and $r_{ds} = 30\text{ k}\Omega$.

$$A_v = \frac{(60)(5 \times 10^3)}{(61)(5 \times 10^3) + (30 \times 10^3)} = 0.895$$

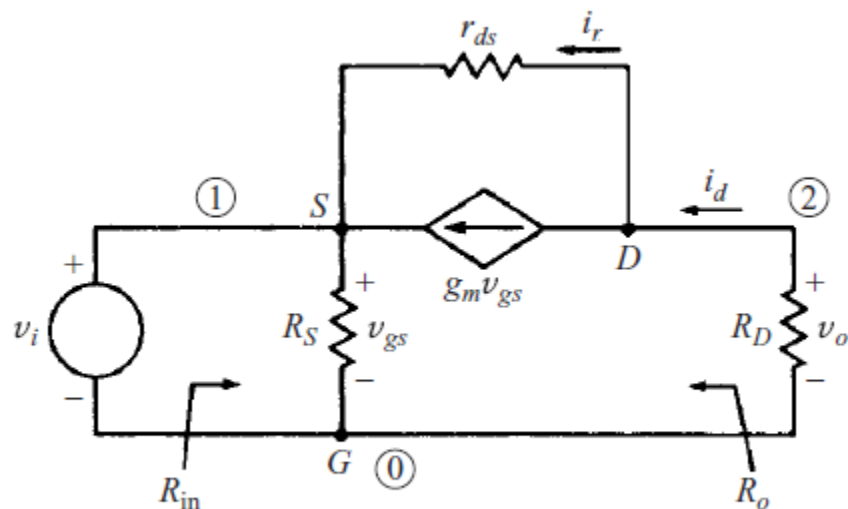


Fig. 7-4 CG small-signal equivalent circuit

By KCL, $i_r = i_d - g_m v_{gs}$. Applying KVL around the outer loop gives

$$v_o = (i_d - g_m v_{gs})r_{ds} - v_{gs}$$

But $v_{gs} = -v_i$ and $i_d = -v_o/R_D$; thus,

$$v_o = \left(-\frac{v_o}{R_D} + g_m v_i \right) r_{ds} + v_i$$

and

$$A_v = \frac{v_o}{v_i} = \frac{(g_m r_{ds} + 1)R_D}{R_D + r_{ds}}$$

let $R_D = 1 \text{ k}\Omega$, $g_m = 2 \times 10^{-3} \text{ S}$, and $r_{ds} = 30 \text{ k}\Omega$.

$$A_v = \frac{(61)(1 \times 10^3)}{1 \times 10^3 + 30 \times 10^3} = 1.97$$

Modeling the Body Effect

$$i_D = K_n(v_{GS} - V_{TN})^2$$

$$V_{TN} = V_{TNO} + \gamma[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}]$$

Back-gate transconductance

$$g_{mb} = \left. \frac{\partial i_D}{\partial v_{BS}} \right|_{Q-pt} = \left. \frac{-\partial i_D}{\partial v_{SB}} \right|_{Q-pt} = - \left(\frac{\partial i_D}{\partial V_{TN}} \right) \cdot \left(\frac{\partial V_{TN}}{\partial v_{SB}} \right) \Big|_{Q-pt}$$

$$\frac{\partial i_D}{\partial V_{TN}} = -2K_n(v_{GS} - V_{TN}) = -g_m$$

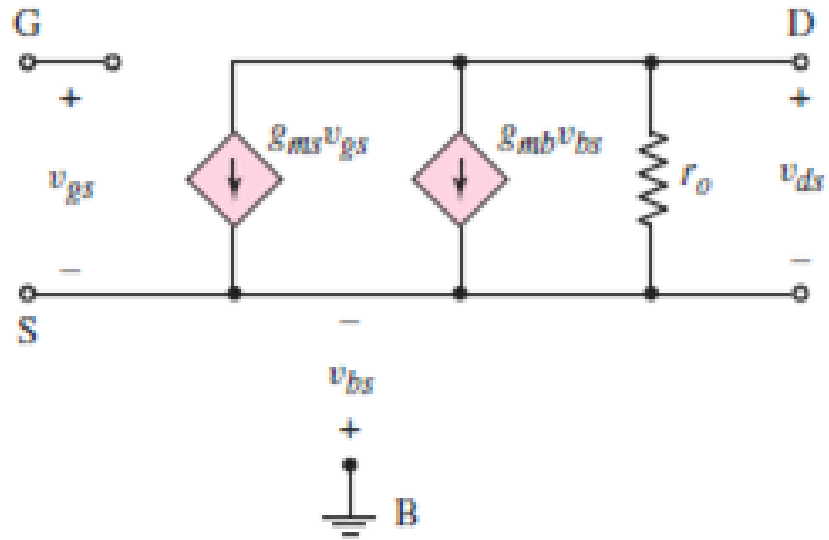
$$\frac{\partial V_{TN}}{\partial v_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + v_{SB}}} \equiv \eta$$

$$g_{mb} = -(-g_m) \cdot (\eta) = g_m \eta$$

$$i_D = f(v_{GS}, v_{DS}, v_{BS})$$

$$i_D = g_m v_{GS} + 1/r_o v_{DS} + g_{mb} v_{BS}$$

$$i_D = g_m v_{GS} + 1/r_o v_{DS} + g_m \eta v_{BS}$$



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Keshav Jasrotia

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Keshav jasrotia- 003

GANAPATI BISWAS

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Ganapati Biswas 001910701090

Rishav Basu

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Sarit Roy Chaudhury

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Souvik Barman

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Arka Chakraborty

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Shubham singh

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Chayan Talukder

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$$A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (f_1/f)^2} \sqrt{1 + (f/f_2)^2}}$$

In the midband, $f_1/f \approx 0$ and $f/f_2 \approx 0$.

Midband: $A_v = A_{v(\text{mid})}$

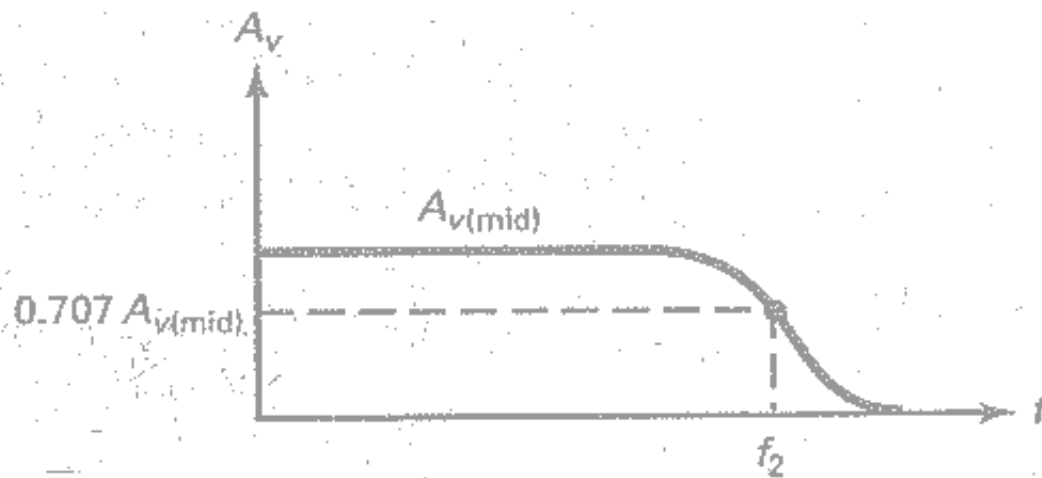
Below the midband, $f/f_2 \approx 0$.

Below midband: $A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (f_1/f)^2}}$

Above midband, $f_1/f \approx 0$.

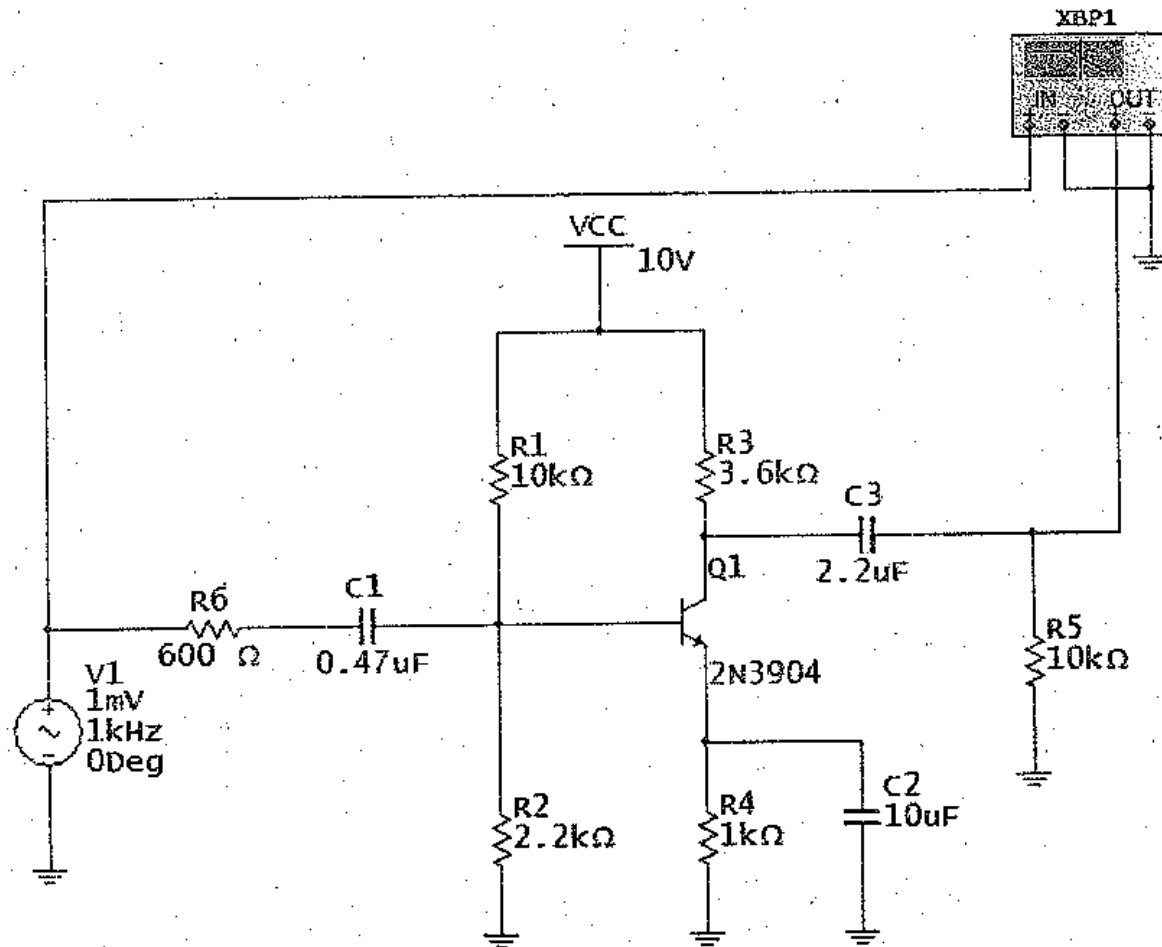
Above midband: $A_v = \frac{A_{v(\text{mid})}}{\sqrt{1 + (f/f_2)^2}}$

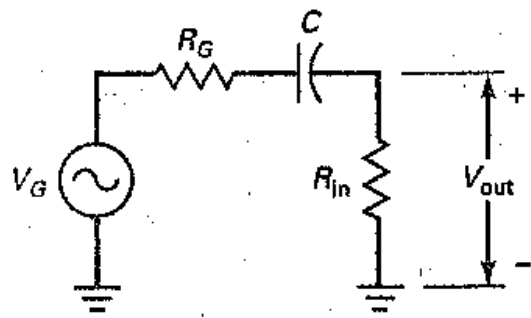
Response of a DC Amplifier



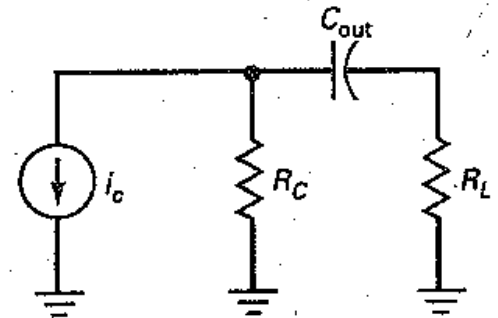
Assignment

Using the circuit values shown in Fig. 16-28a, calculate the low-cutoff frequency for each coupling and bypass capacitor. Compare the results to a measurement using a Bode plot. (Use 150 for the dc and ac beta values.)

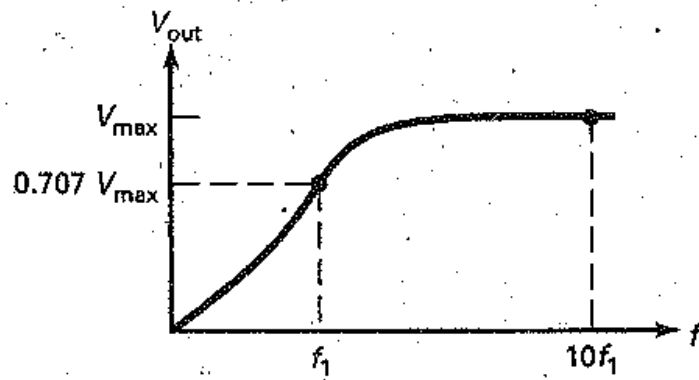




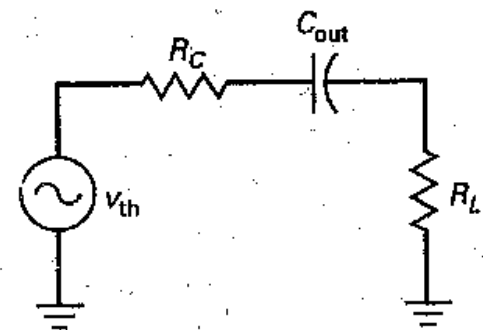
(a)



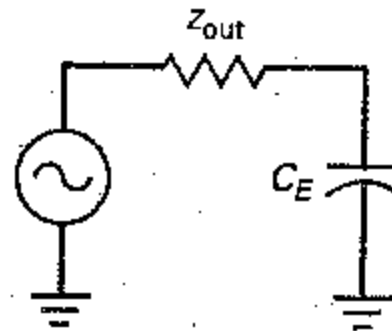
(a)



(b)

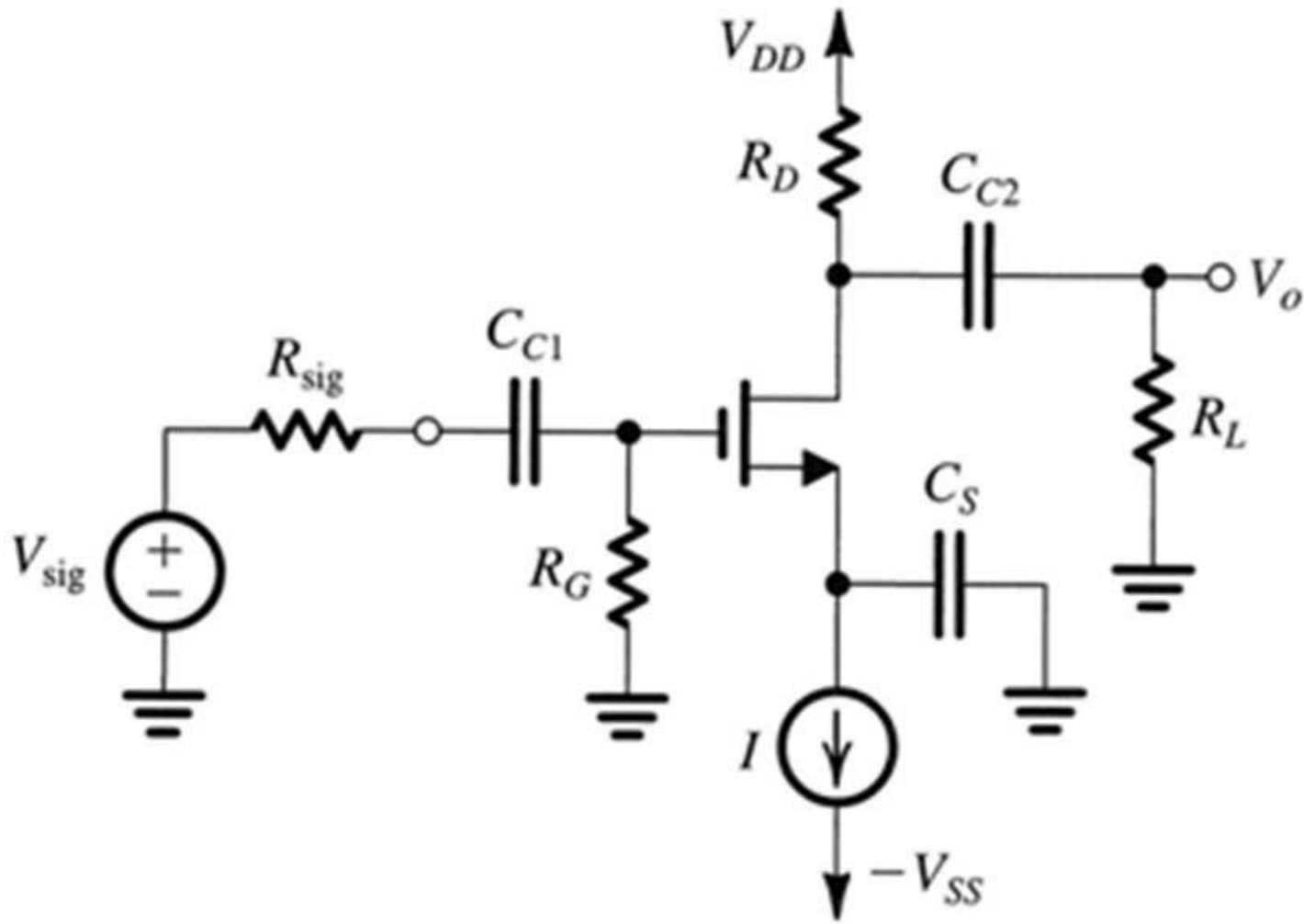


(b)

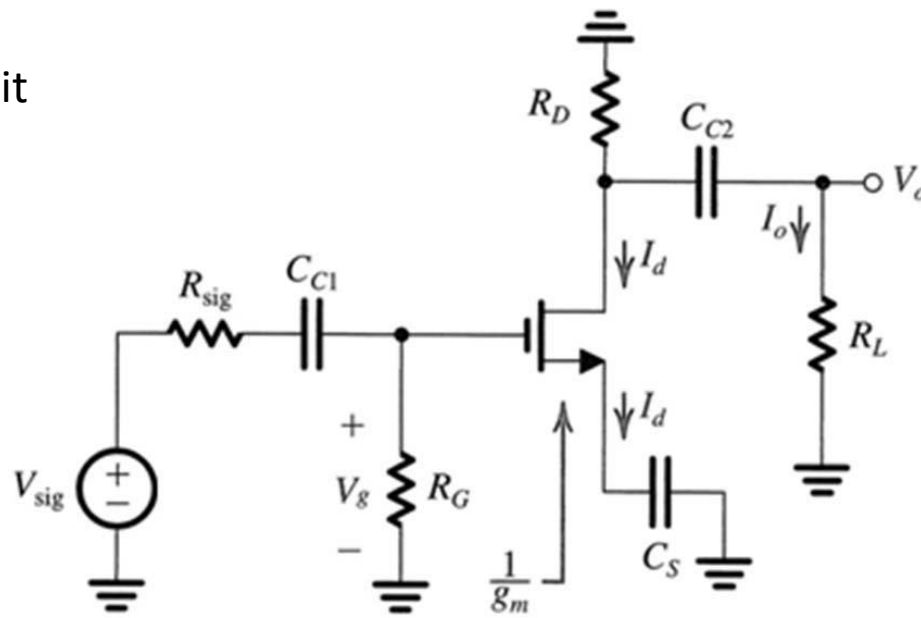


(c)

Frequency Analysis of FET Stages



Ac equivalent circuit



$$V_g = V_{sig} \frac{R_G}{R_G + \frac{1}{sC_{C1}} + R_{sig}} = V_{sig} \frac{R_G}{R_G + R_{sig}} \frac{s}{s + \frac{1}{C_{C1}(R_G + R_{sig})}}$$

$$\omega_{P1} = \frac{1}{C_{C1}(R_G + R_{sig})}$$

$$I_d = \frac{V_g}{\frac{1}{g_m} + \frac{1}{sC_S}} = g_m V_g \frac{s}{s + \frac{g_m}{C_S}}$$

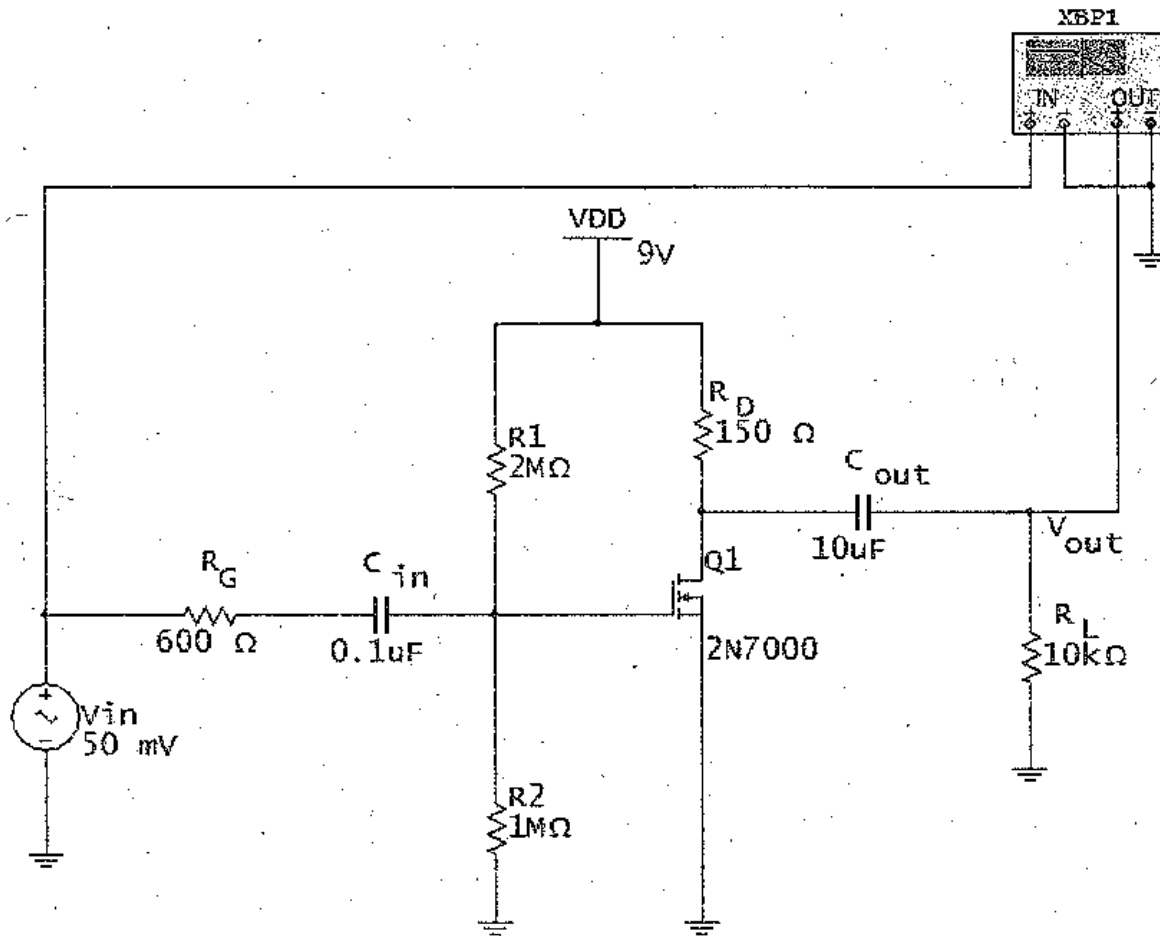
$$\omega_{P2} = \frac{g_m}{C_S}$$

$$V_o = I_o R_L = -I_d \frac{R_D}{R_D + \frac{1}{sC_{C2}} + R_L} R_L = -I_d \frac{R_D R_L}{R_D + R_L} \frac{s}{s + \frac{1}{C_{C2}(R_D + R_L)}}$$

$$\omega_{P3} = \frac{1}{C_{C2}(R_D + R_L)}$$

$$\frac{V_o}{V_{sig}} = -\frac{g_m R_G (R_D \parallel R_L)}{R_G + R_{sig}} \left(\frac{s}{s + \omega_{P1}} \right) \left(\frac{s}{s + \omega_{P2}} \right) \left(\frac{s}{s + \omega_{P3}} \right)$$

$$A_M = -\frac{g_m R_G (R_D \parallel R_L)}{R_G + R_{sig}}$$



(a)

Fig. 16-32 shows an E-MOSFET common-source amplifier circuit using voltage-divider bias. Because of the very high input resistance of the MOSFET, the resistance R facing the input coupling capacitor is:

$$R = R_G + R_1 \parallel R_2 \quad (16-36)$$

and the input coupling cutoff frequency is found by:

$$f_1 = \frac{1}{2\pi RC}$$

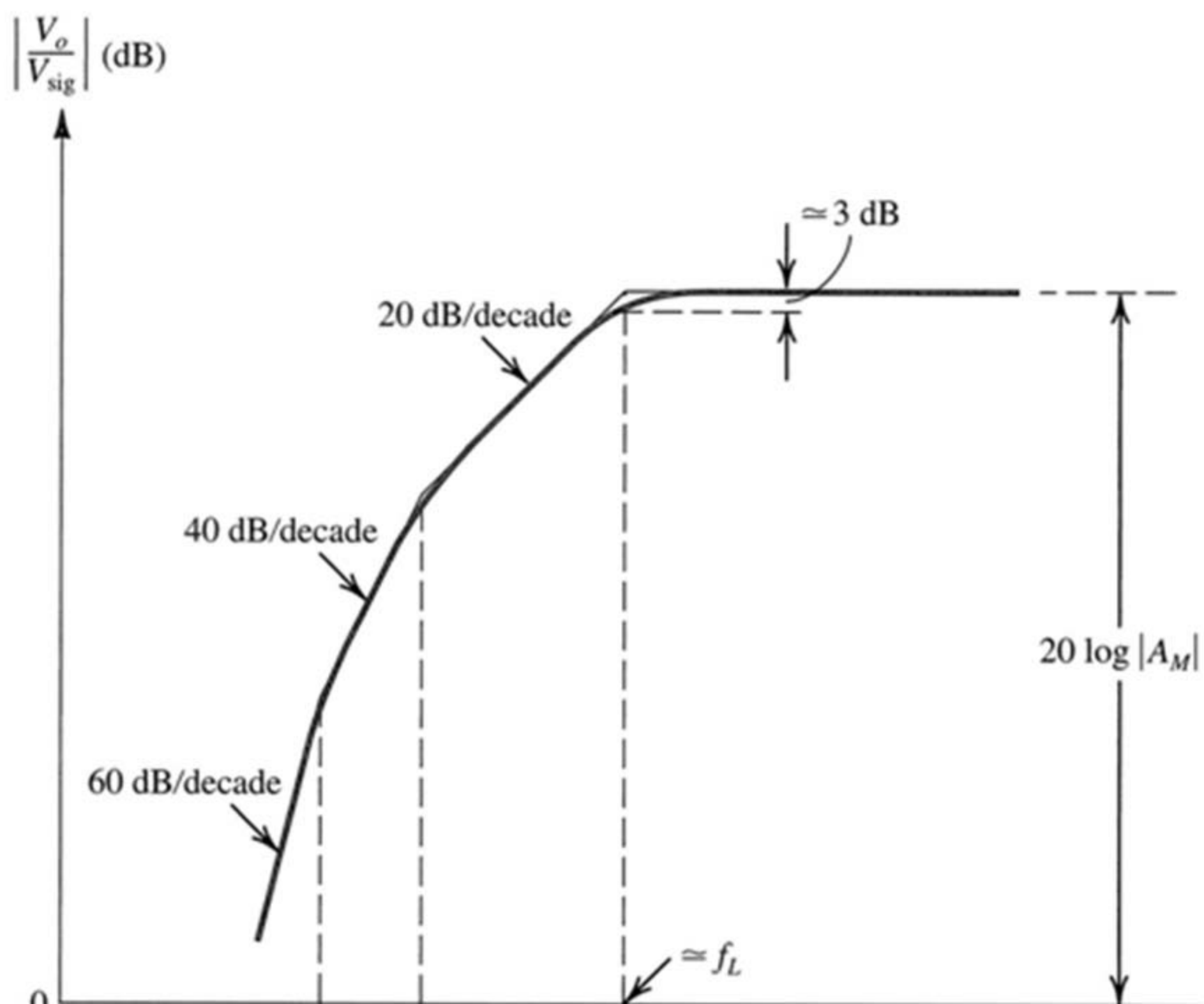
The output resistance facing the output coupling capacitor is:

$$R = R_D + R_L$$

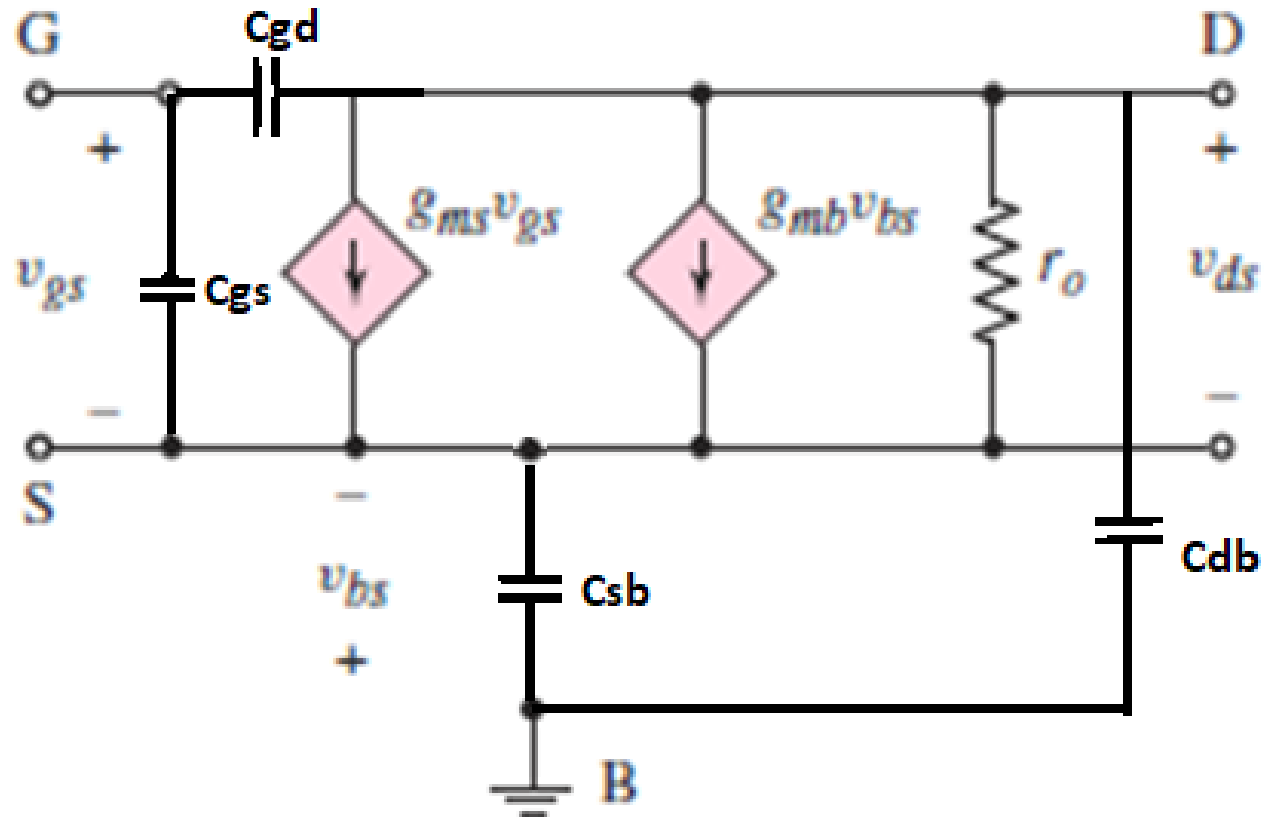
and the output coupling cutoff frequency is found by:

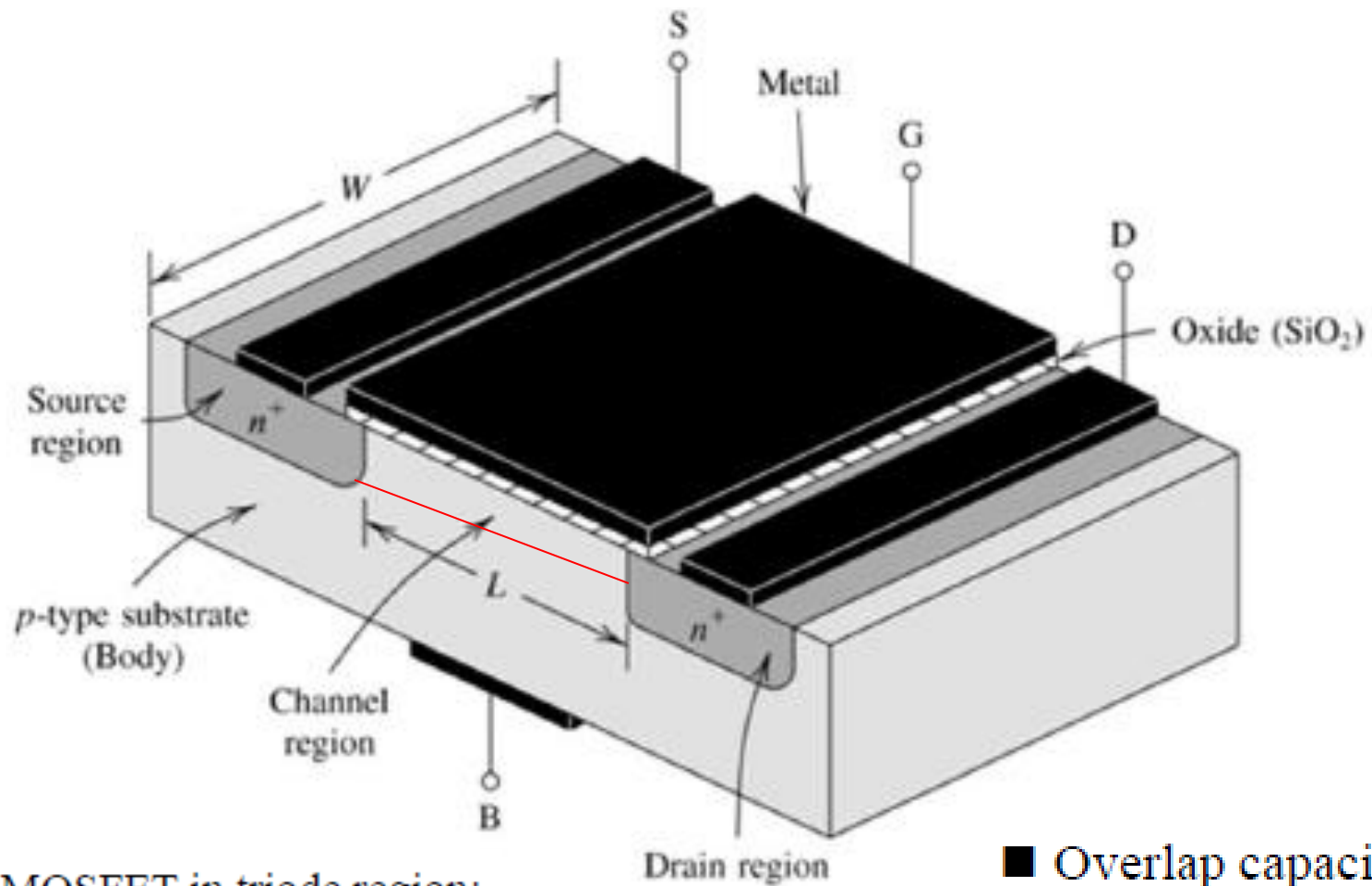
$$f_1 = \frac{1}{2\pi RC}$$

As you can see, the low-frequency analysis of the FET circuit is very similar to the BJT circuit. Because of the very high input resistance of the FET, larger voltage-divider-resistor values can be used. This results in being able to use a much smaller input-coupling capacitor.



High frequency Analysis





■ MOSFET in triode region:

$$C_{gs} = C_{gd} = \frac{1}{2}WLC_{ox} + C_{ov} \quad V_{DS} \text{ is small}$$

■ Overlap capacitance:

$$C_{ov} = WL_{ov}C_{ox}$$

■ MOSFET in saturation region:

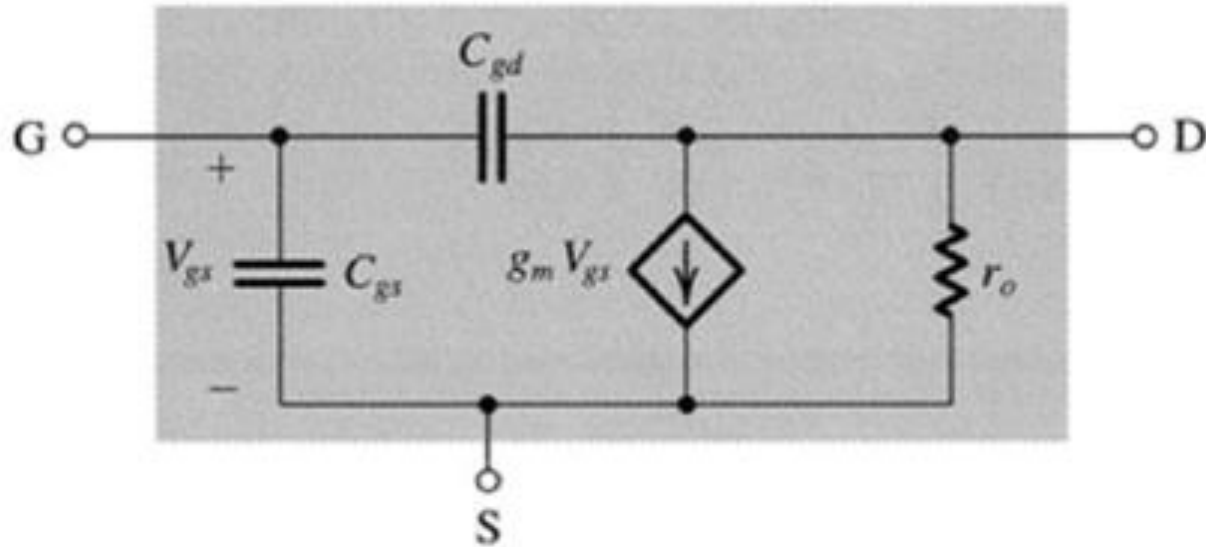
$$C_{gs} = \frac{2}{3}WLC_{ox} + C_{ov} \quad C_{gd} = C_{ov}$$

■ MOSFET in cutoff region:

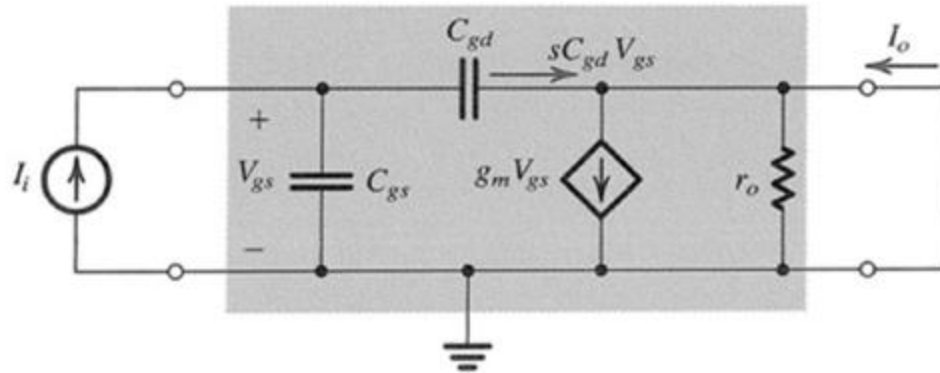
$$C_{gs} = C_{gd} = C_{ov} \quad C_{gb} = WLC_{ox}$$

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + V_{SB} / V_0}}$$

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + V_{DB} / V_0}}$$



The unity-gain frequency (f_T)



$$I_o = g_m V_{gs} - sC_{gd} V_{gs} \approx g_m V_{gs}$$

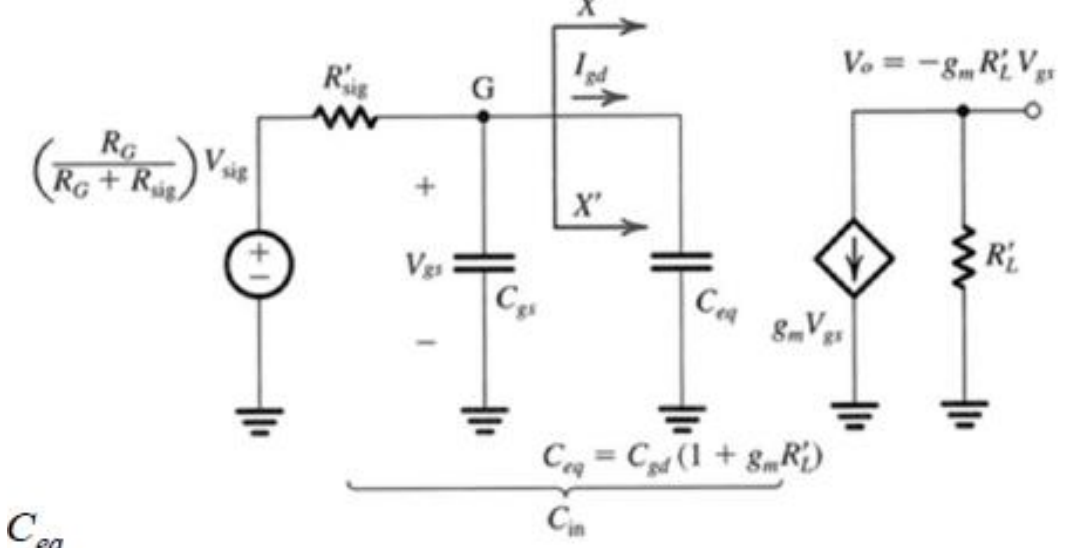
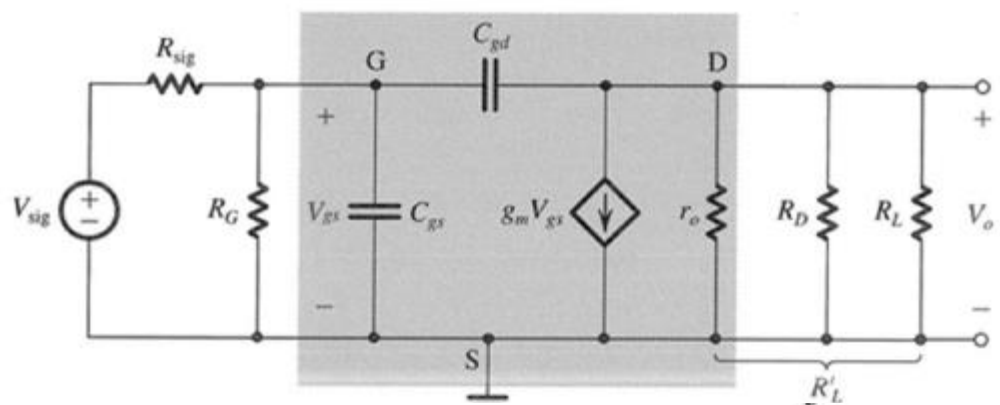
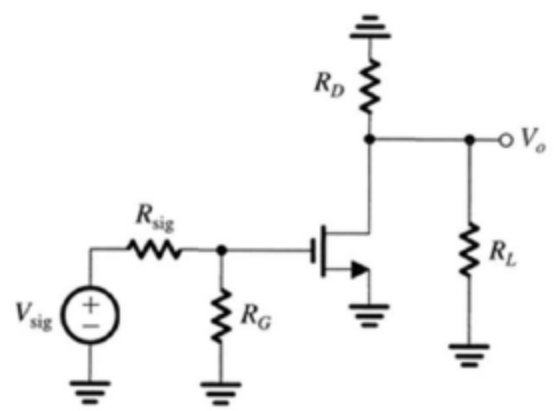
$$V_{gs} = \frac{I_i}{s(C_{gs} + C_{gd})}$$

$$\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})}$$

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gd}}$$

$$f_T = \frac{1}{2\pi} \frac{\mu_n C_{ox} (W/L) V_{OV}}{C_{gs} + C_{gd}} \approx \frac{3\mu_n V_{OV}}{4\pi L^2}$$

$$V_{OV} = V_{GS} - V_{TH}$$



C_{eq}

$$\frac{V_o}{V_{sig}} = - \frac{\left[\left(\frac{R_G}{R_{sig} + R_G} \right) g_m R'_L \right]}{1 + s \{ R'_{sig} [(1 + g_m R'_L) C_{gd} + C_{gs}] \}} = - \frac{A_M}{1 + \frac{s}{\omega_H}}$$

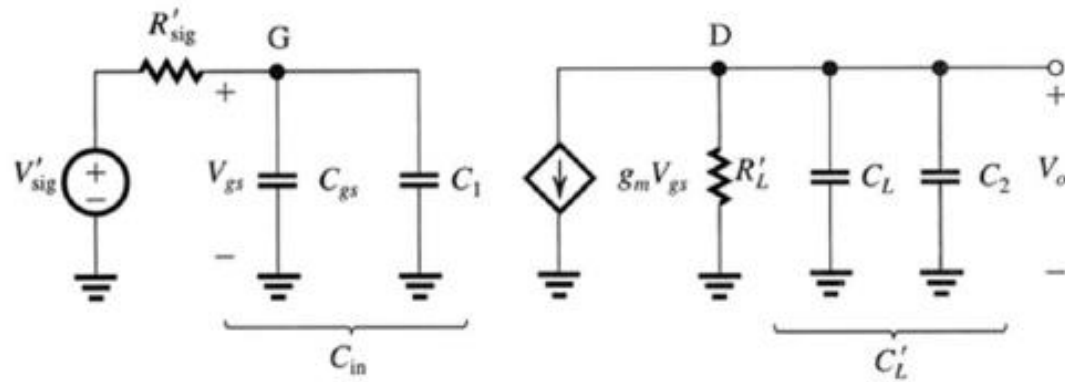
$$A_M = - \frac{R_G}{R_G + R_{sig}} (g_m R'_L)$$

$$\omega_H = \{ R'_{sig} [(1 + g_m R'_L) C_{gd} + C_{gs}] \}^{-1}$$

$$= 1/R'_{sig}$$

$$C_{in}$$

$$R'_{sig} = R_G || R_{sig}$$



$$\frac{V_o}{V_{sig}} = \left(-g_m R'_L \frac{R_G}{R_G + R_{sig}} \right) \frac{1}{(1 + \omega / \omega_{p1})(1 + \omega / \omega_{p2})}$$



$$1/\omega_{p1} = C_{in} R'_{sig} = [C_{gs} + C_{gd}(1 + g_m R'_L)]$$

$$1/\omega_{p2} = C'_L R'_L \approx (C_L + C_{gd}) R'_L$$

$$\omega_H = \frac{1}{\sqrt{1/\omega_{p1}^2 + 1/\omega_{p2}^2}} \approx \omega_{p1}$$

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Abhijit Deogharia

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