Cadence Virtuoso

Custom IC Design Using Cadence Tools

INTRODUCTION

- Cadence design system provides high performance tools for analog/digital implementation, custom IC design, IC packaging & co-design and similar solution.

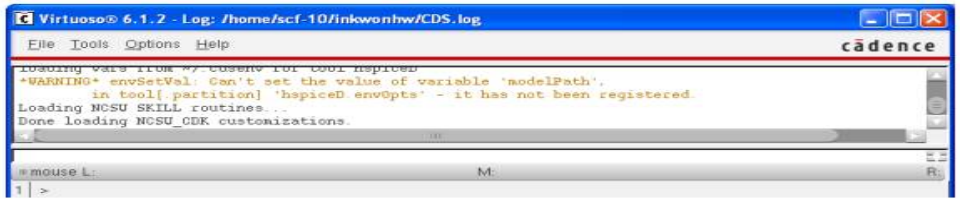
- “Virtuoso analog implementation technology is the industry leader in its market segment. As such, it is a priority at Cadence to continually enhance the Virtuoso suite and deliver the sophisticated technology and usability levels our customers ask for. Virtuoso offer greater capacity, performance, and usability to reduce overall design time while ensuring high-quality production of analog/mixed-signal ICs and SoCs.”

Introduction To Cadence Virtuoso

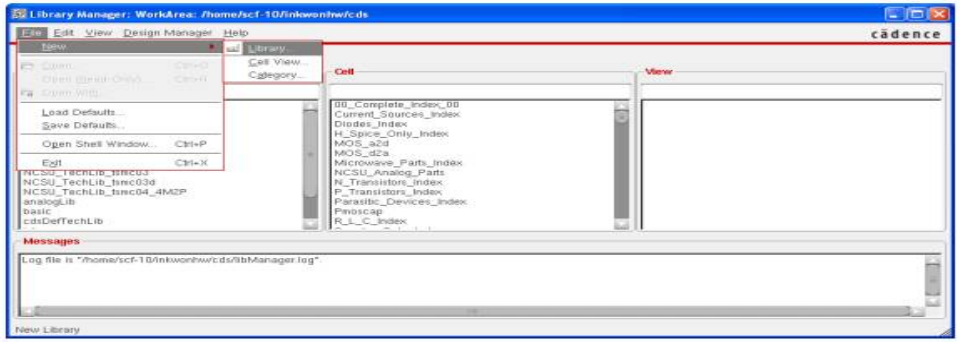
- Cadence virtuoso tool is installed in the CentOS operating system . A pre-set working library has been created for quick access. Open terminal inside the directory and type the following
- **Csh**(enter)
- **Source/cad/cshrc(**enter)
- **Virtuoso(**enter)
- The Virtuoso tool will be opened. Go to the **Library Manager** for navigating the pre-installed directories and creating custom directory.
- Pre-installed directories:
- **gpdk045/gpdk090/gpdk180/tsmc180** : core cell library
- **PDK** : stander cell library
- **analogLIb** : voltage/current/cap/res library
- Create a new Library:
- File/new library/<NAME>(press ok)
- Attach to an existing library (e.g. gpdk180)(press ok) # A new library named NAME will be created

Create Library

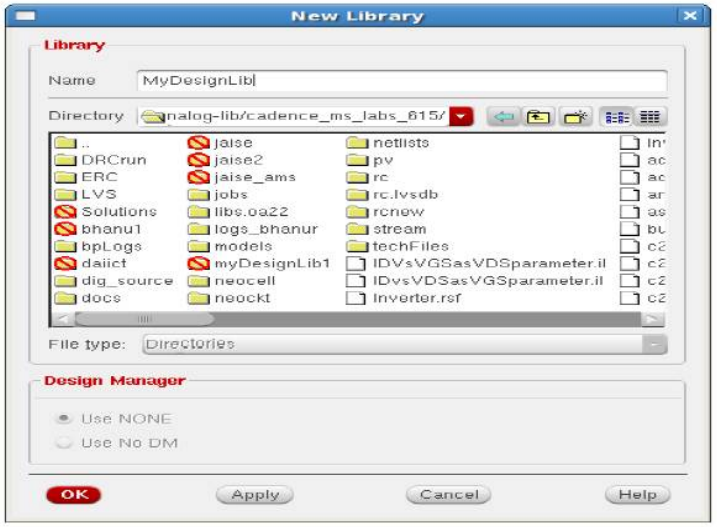
A. Tools → Library Manager



B. File → New → Library

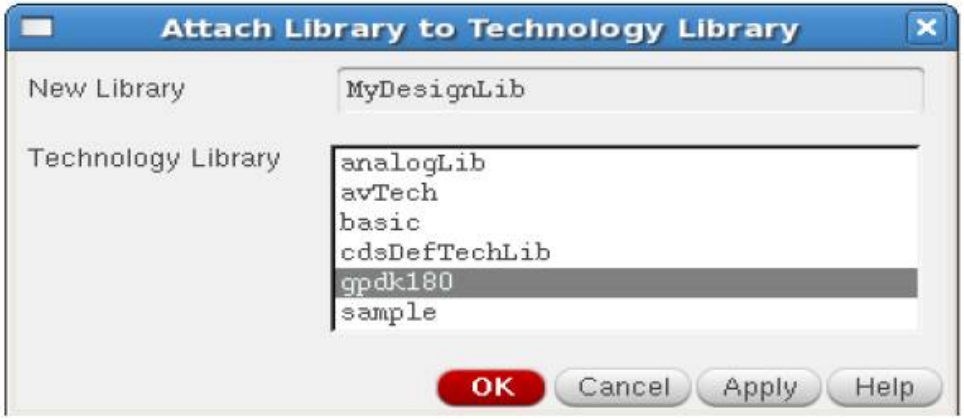


C.

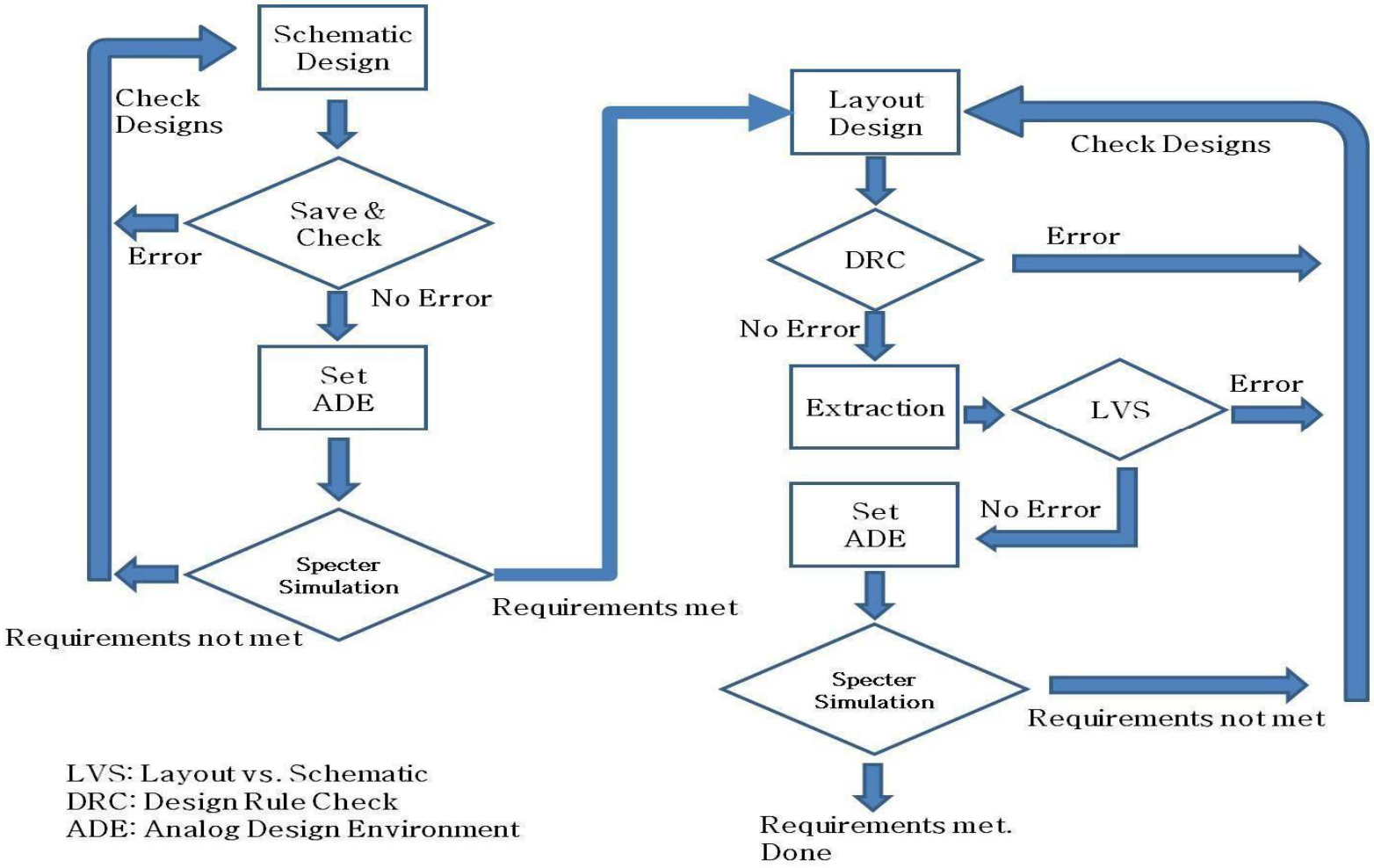


D.

E.



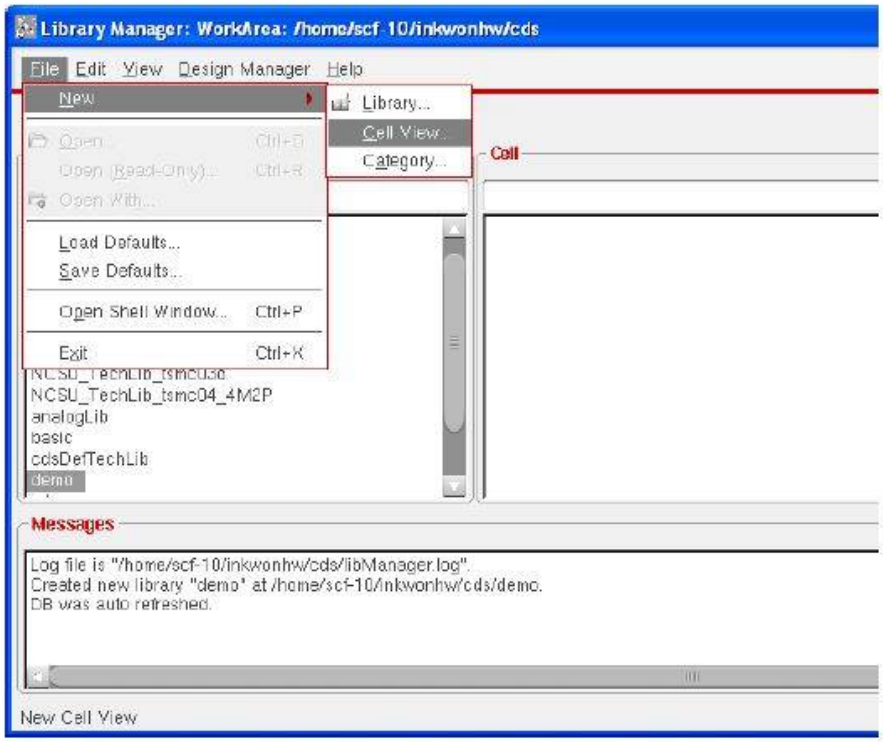
Overall Design Flow

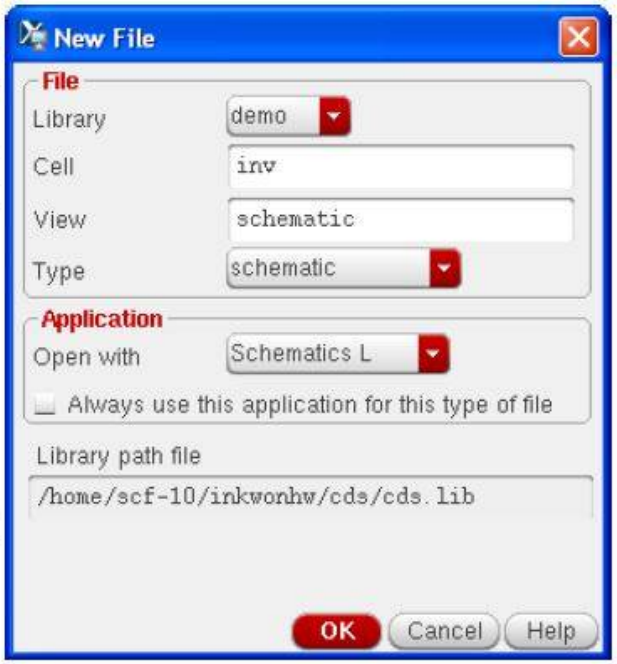


LVS: Layout vs. Schematic
DRC: Design Rule Check
ADE: Analog Design Environment

Create a New Schematic

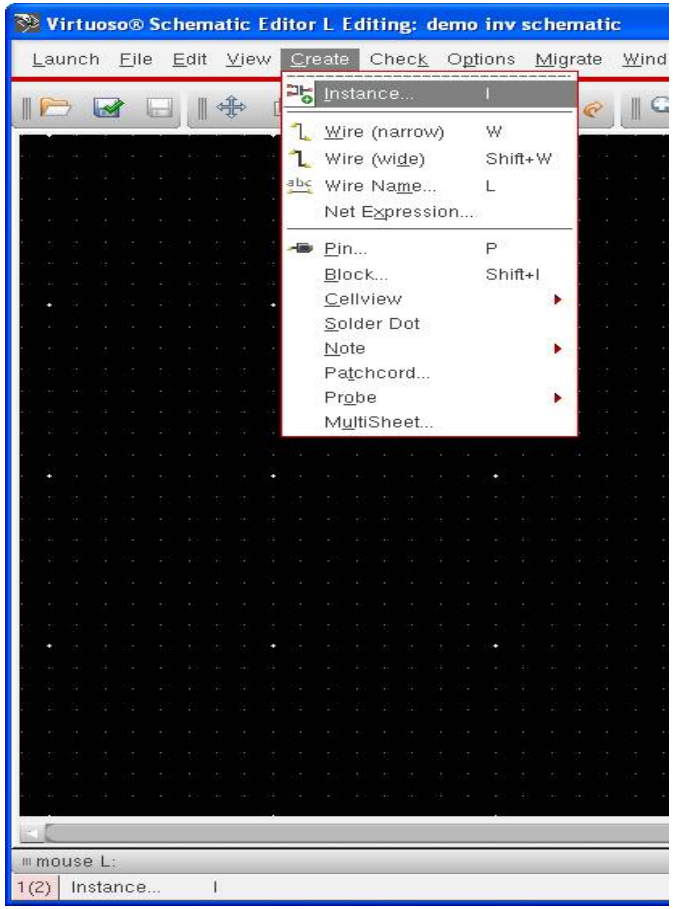
- CREATE CELL VIEW: select the library File-New – Cell view(select the type as schematic) (press **OK**) .# A window with black background and white dots will open where the circuit is drawn

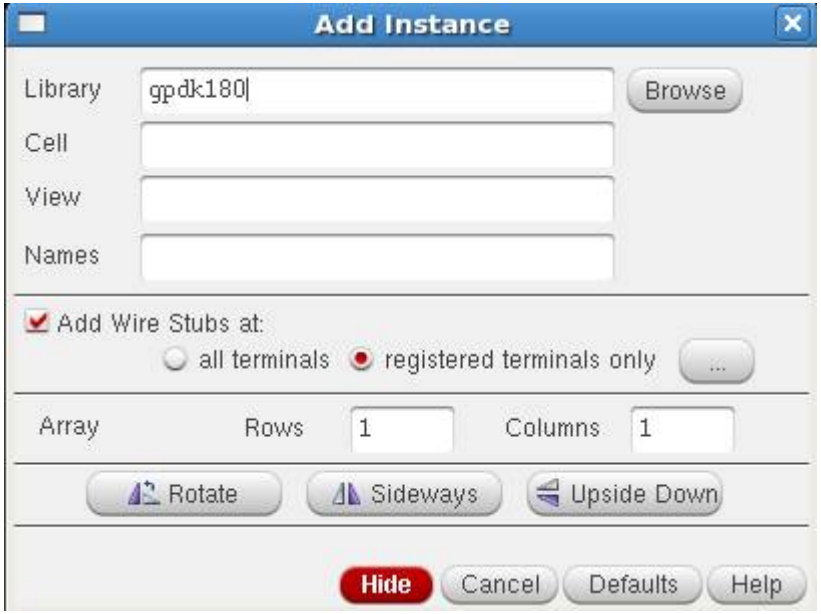




Draw a Schematic

- ADD COMPONENTS: In the Inverter Schematic window Create-> Instance or press I then Add instance window will open, from where we can select the component.

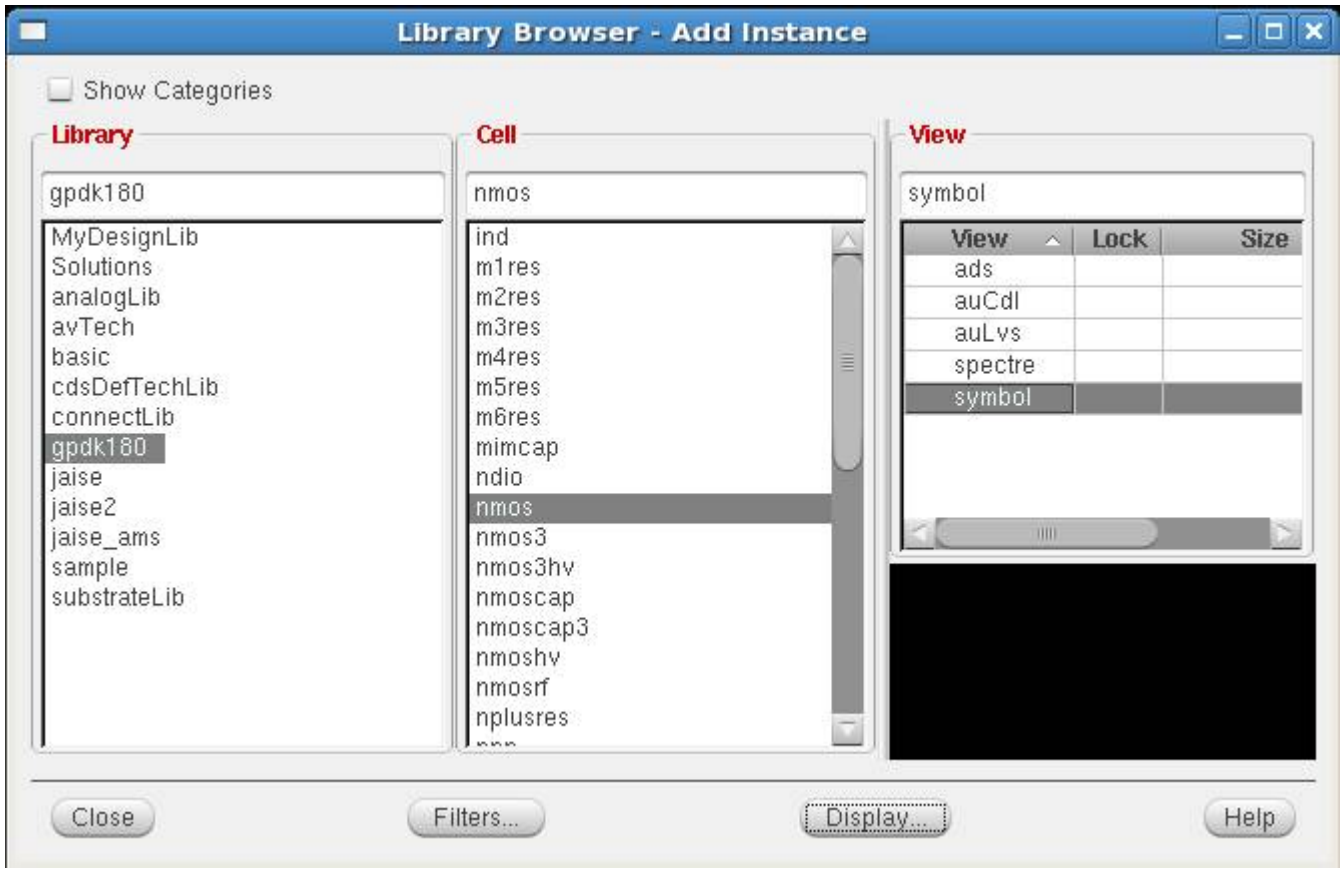




Draw a Schematic

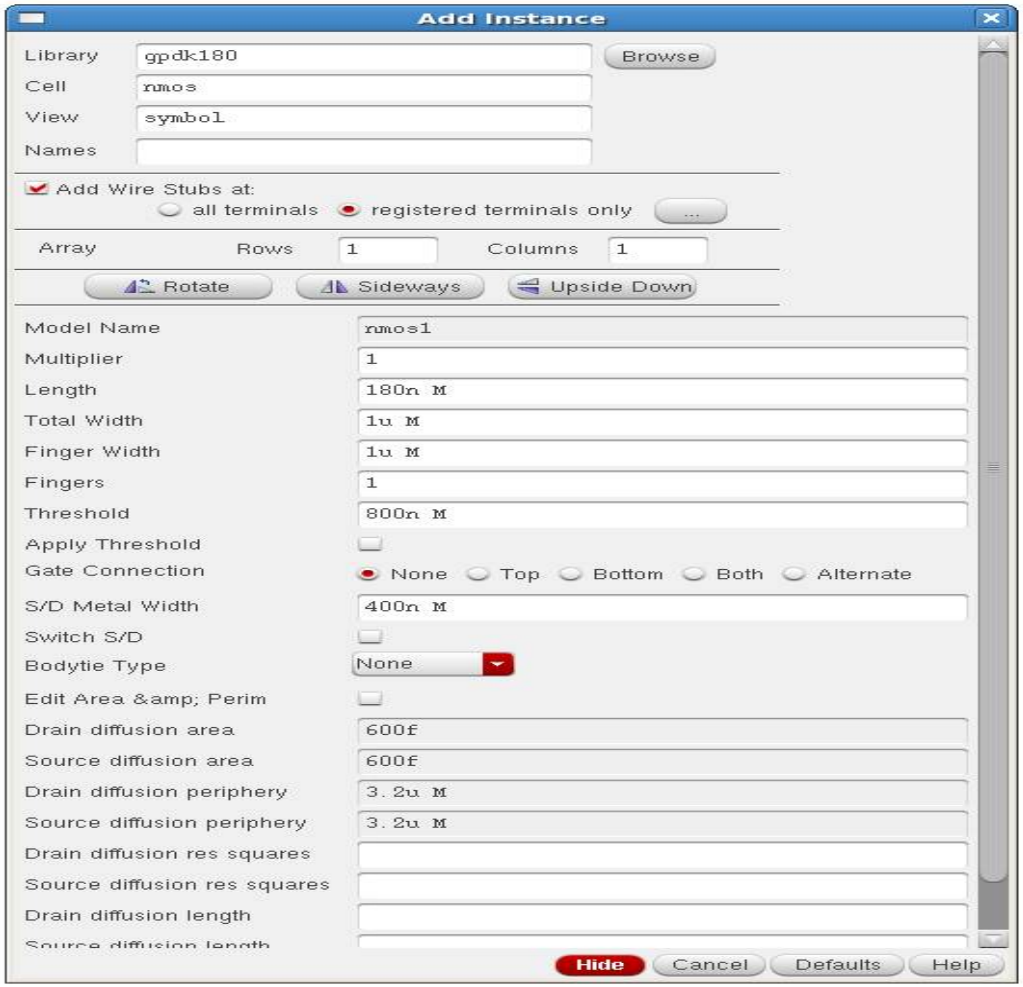
(**Adding Components to schematic**)

- Click on Browse in Add instance window. This opens up a Library browser from which you can select components and the **symbol view.**



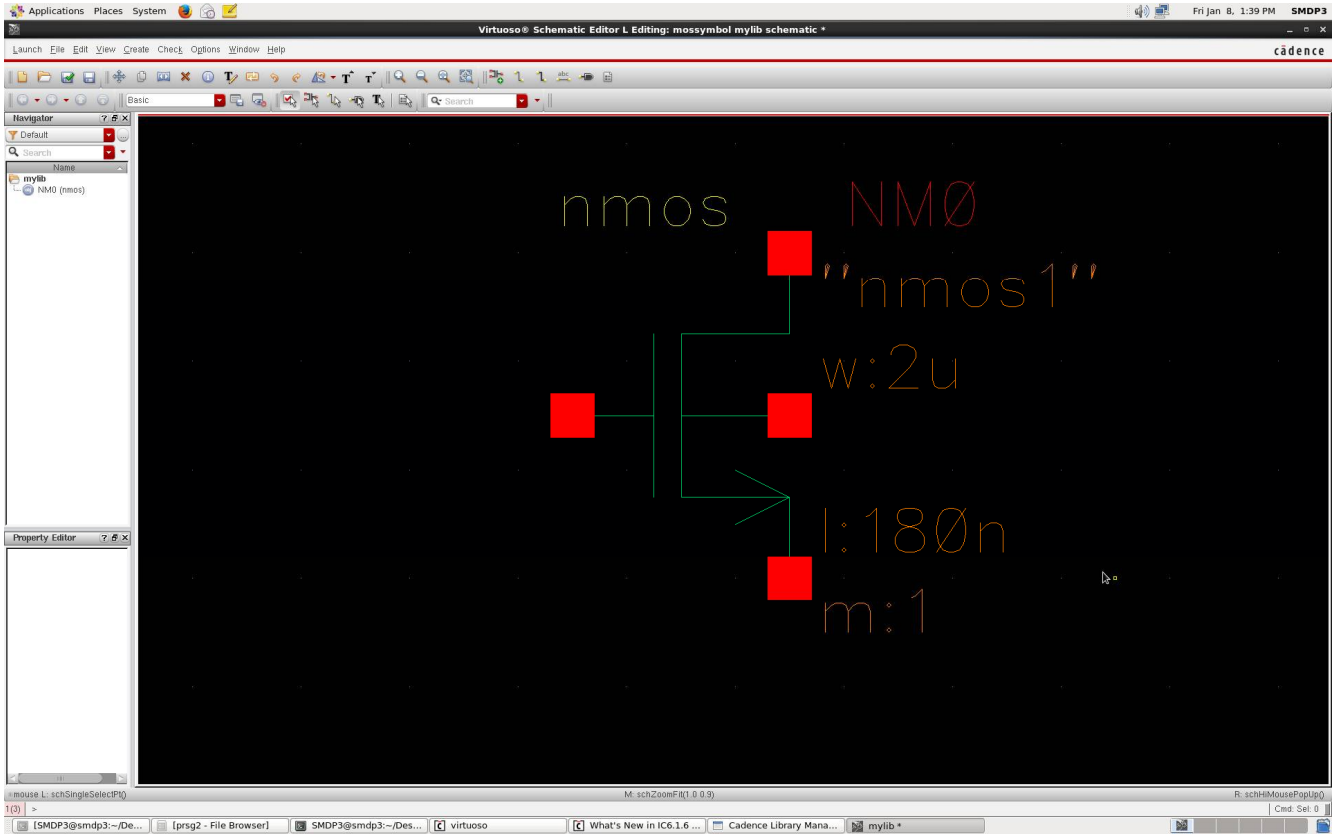
Adding Components to schematic

- update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.
- Instantiating the nmos symbol is shown below as an example.
- After you complete the Add Instance form, move your cursor to the Schematic window and **left click to place a component.**
- If you place a component with the wrong parameter values, use the **Edit— Properties— Objects command to change the parameters (**for edit select the component press Q **)**



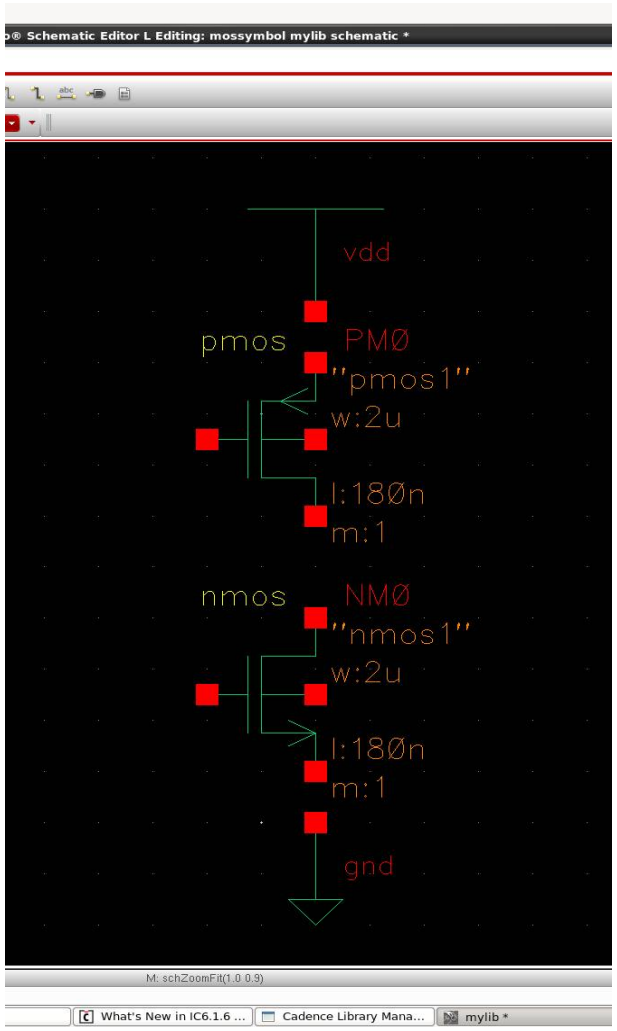
Draw a Schematic

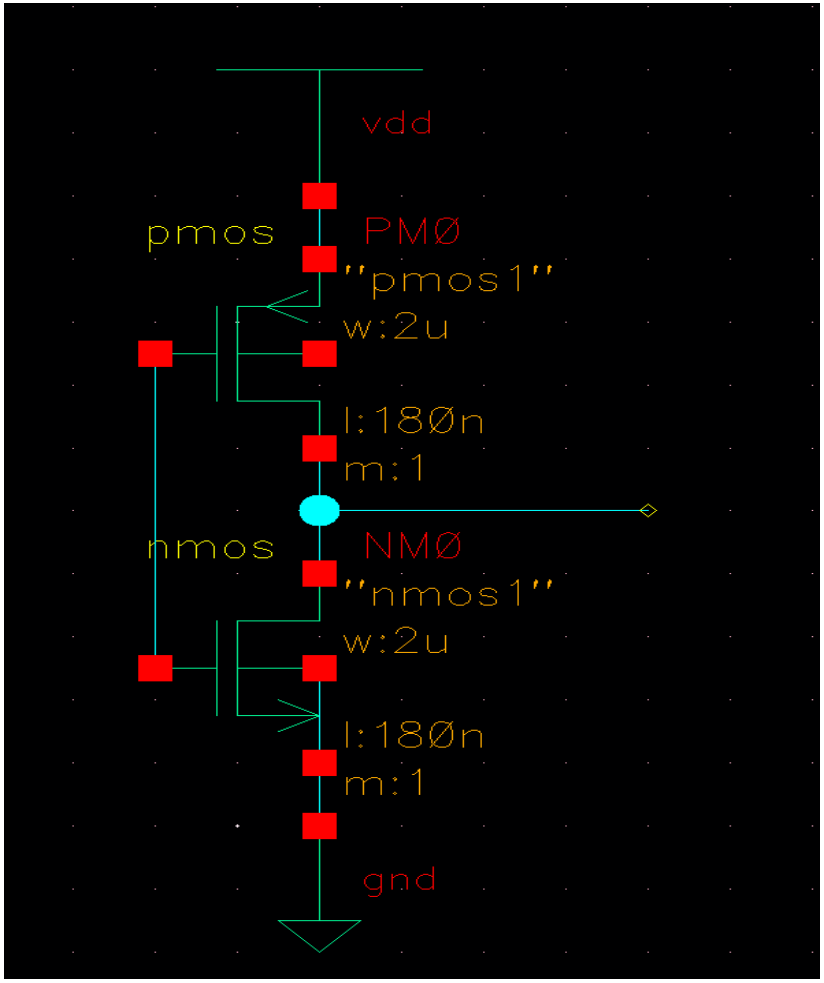
- After you complete the Add Instance form, move your cursor to the Schematic window and **left click to place a component.** The component is placed as shown below



Draw a Schematic

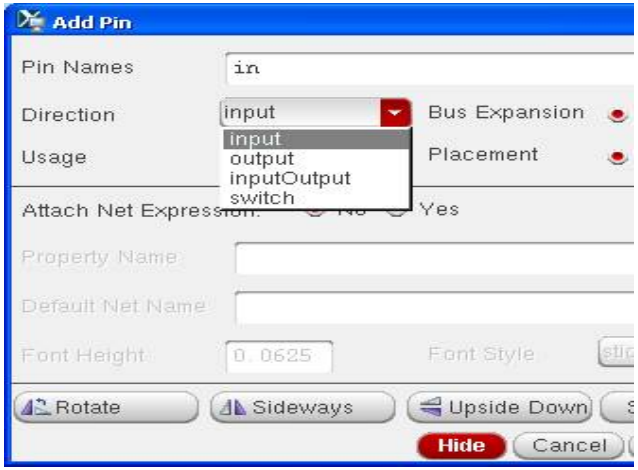
- ADD WIRES: Create-> Wire or press W and join the nodes to be connected.

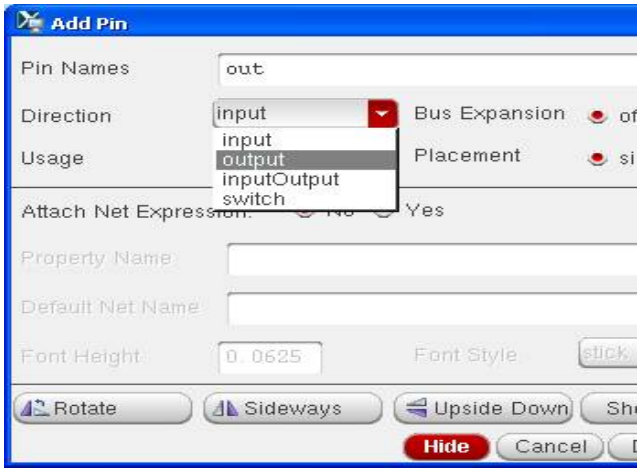


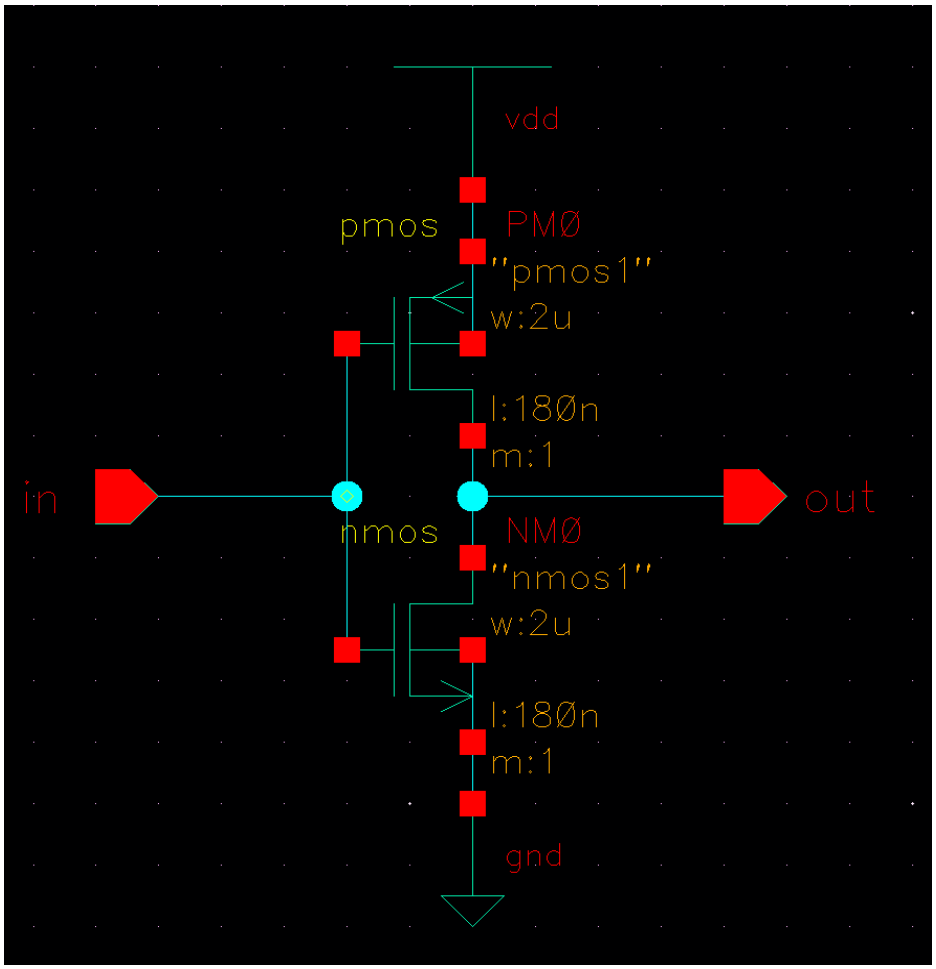


Draw a Schematic

- ADD PINS: Create-> Pin or press P, select the type of pins to be used and place them as required.

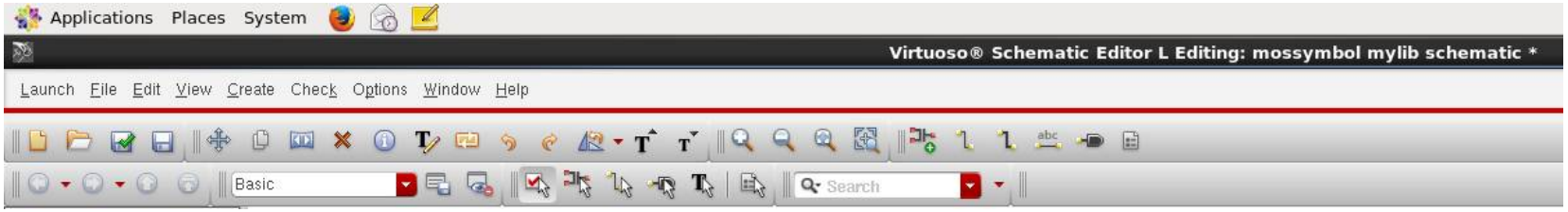


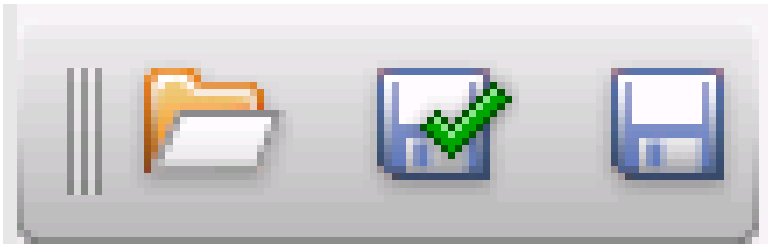




Check and Save

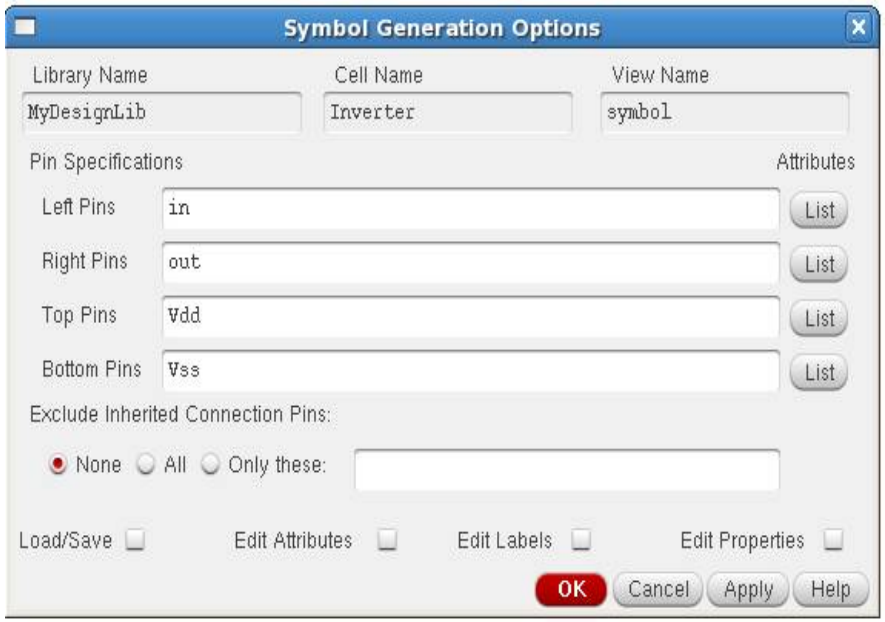
- Click the **Check and Save icon in the schematic editor window**.





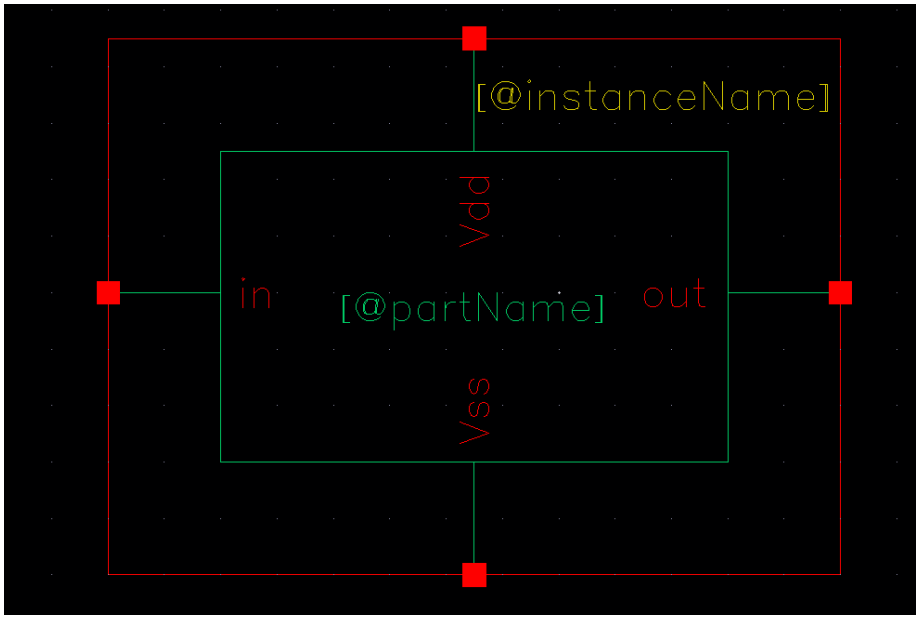
Symbol Creation

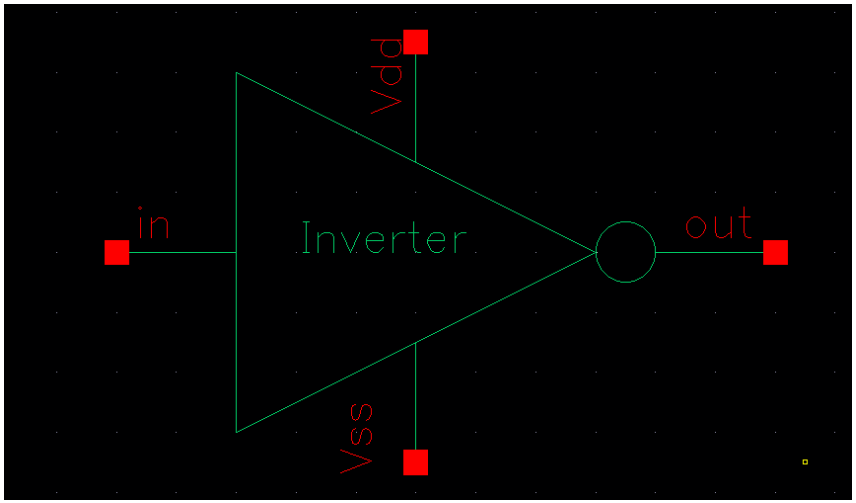
- CREATE SYMBOL: Create -> Cell View -> From Cell View. A From Cell View window opens for symbol creation. Click OK. The Symbol Generation options window opens, where pins are to be arranged. Click OK.



Symbol Creation

- After the Symbol Generation options window closes, a new window displays with an automatically created Inverter symbol as shown.

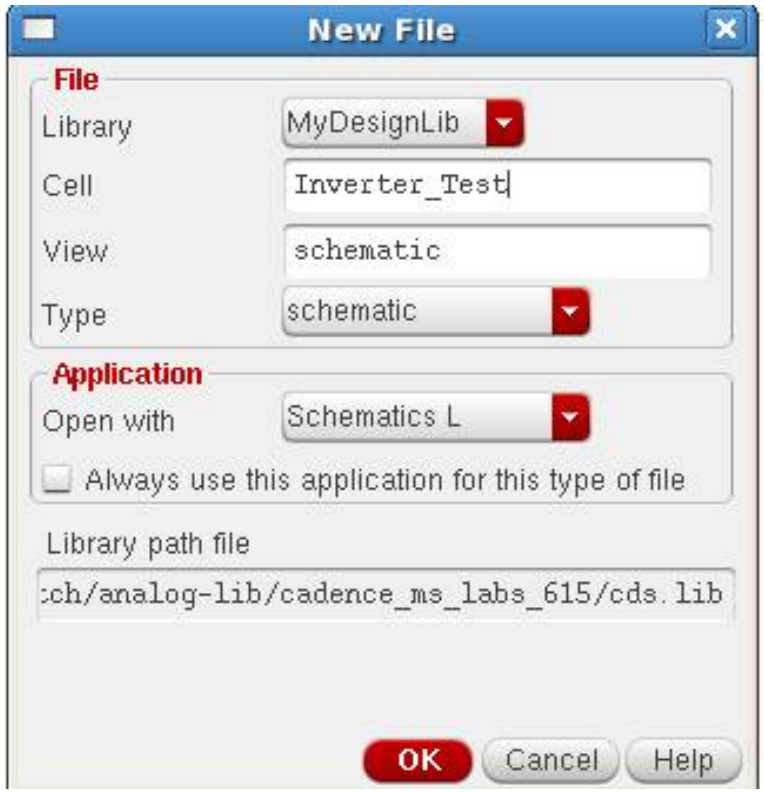




• Modify the inverter symbol to look like an Inverter gate symbol using the option Create -> Shape (as available in the window like circle, polygon, etc).

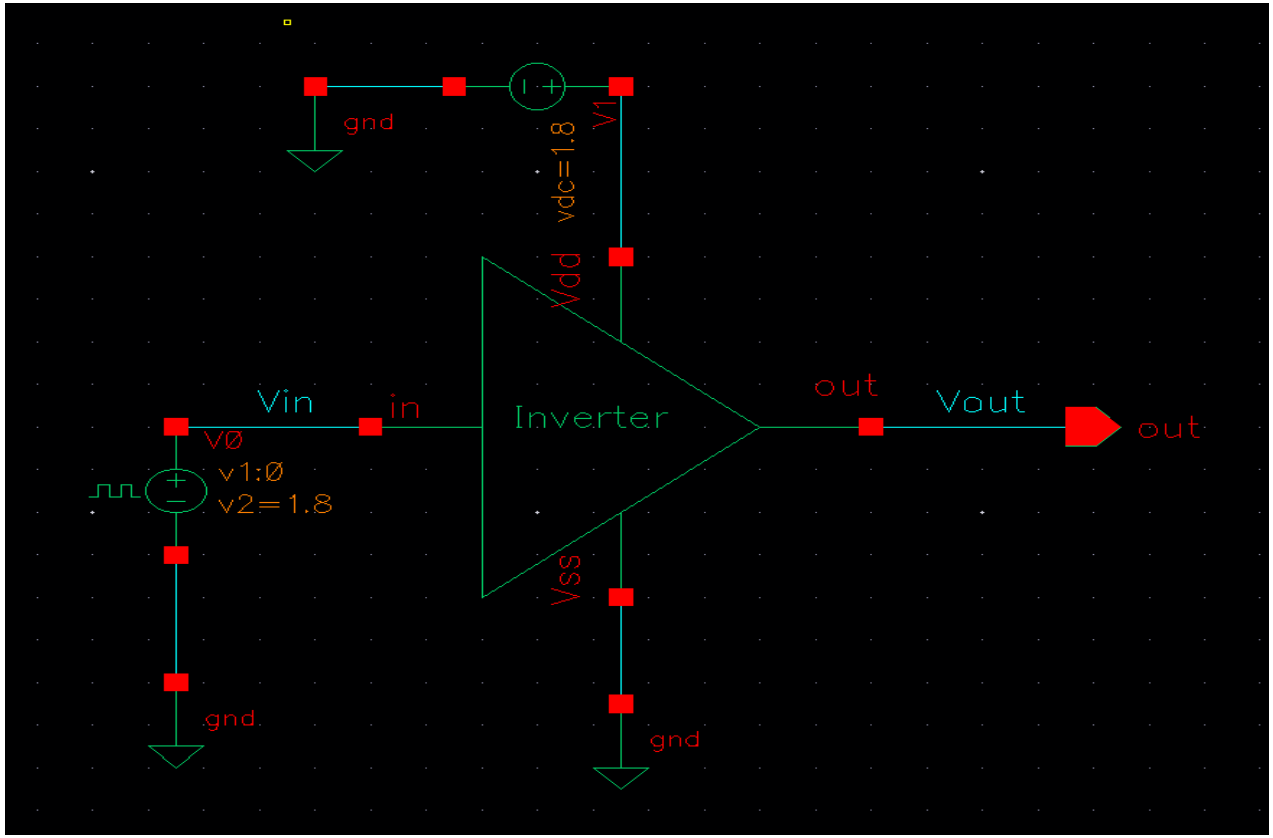
Test Circuit Creation

- CREATE TEST CIRCUIT: Select the library. File-> New–> Cell view(select the type as schematic) (press **OK**).



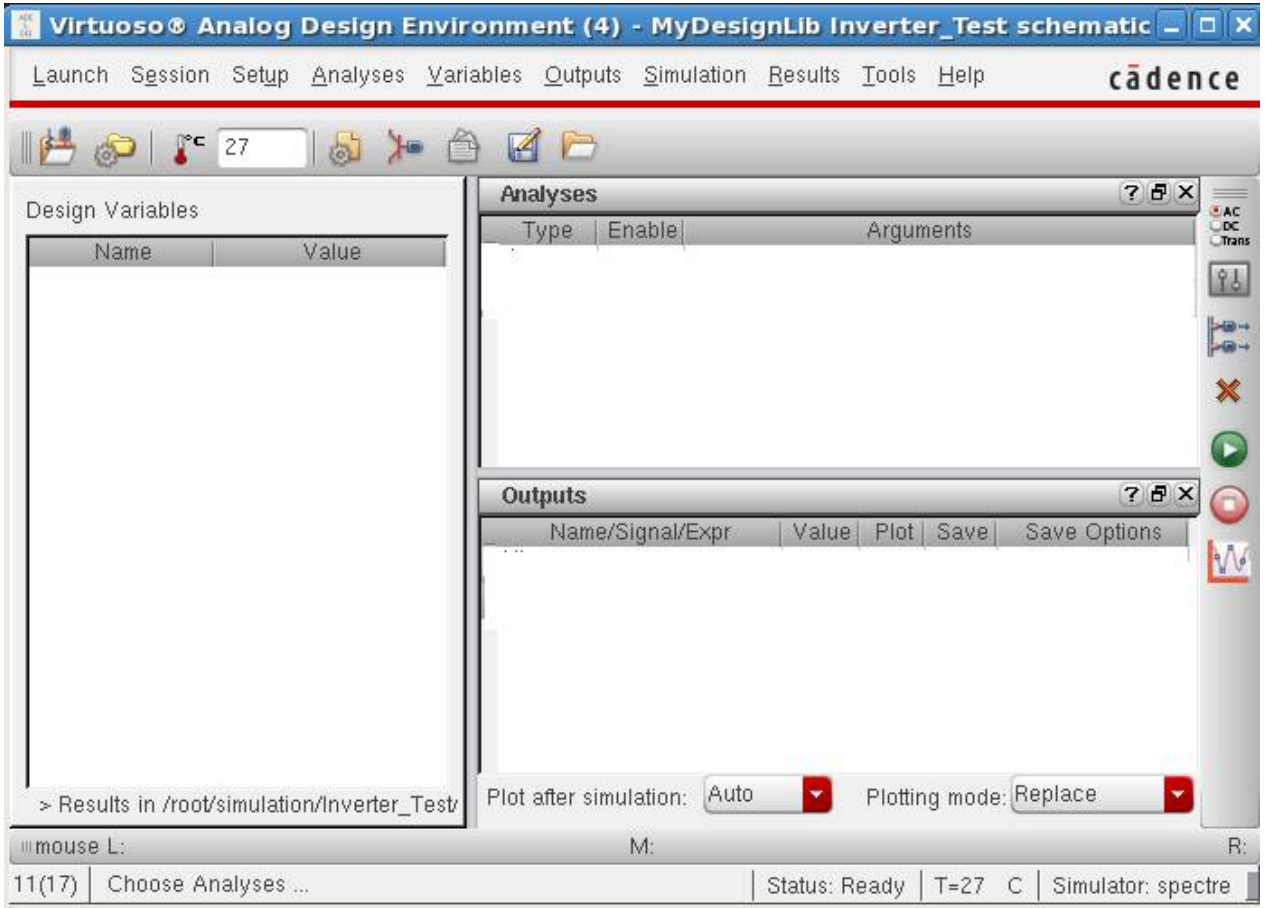
Test Circuit Design

- CREATE TEST DESIGN: Design the test circuit for the inverter by calling the inverter symbol created in the same process as the components were called.



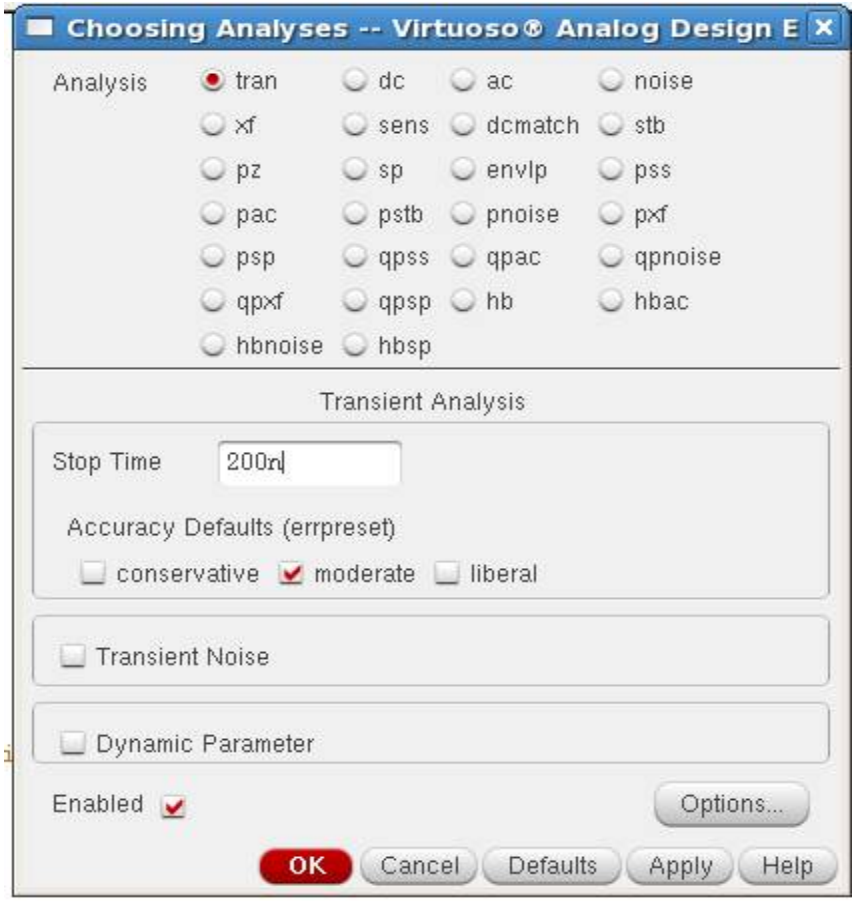
Simulation

- SIMULATION: In the Inverter Test schematic window, click Launch–> ADE L. The Virtuoso Analog Design Environment (ADE) simulation window opens.



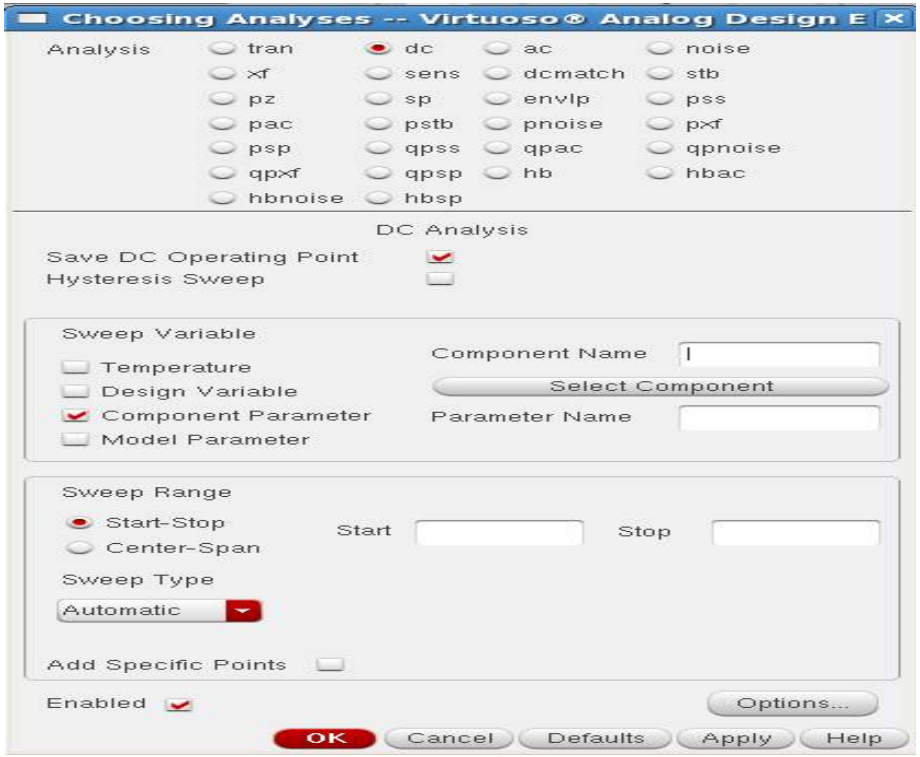
Transient Analysis

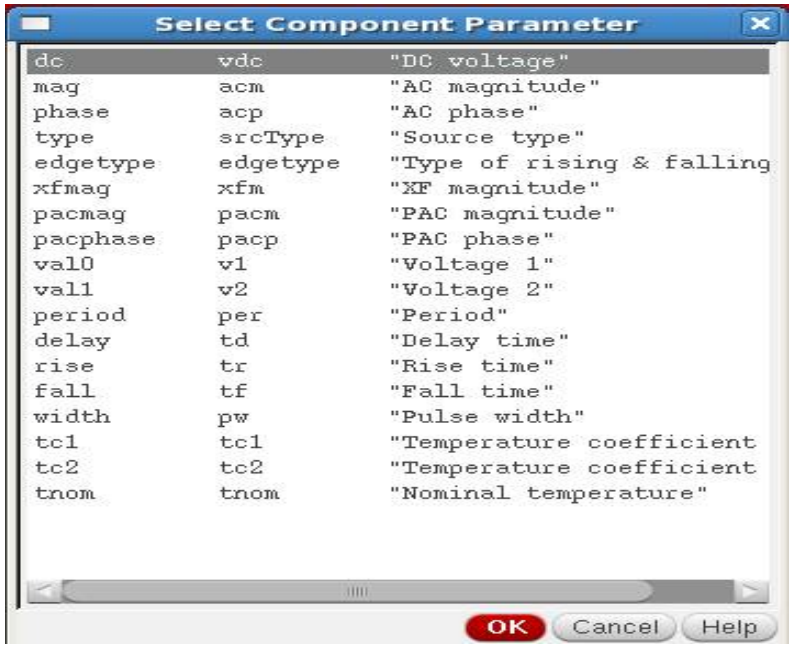
- TRANSIENT ANALYSIS: In ADE window, Analysis-> Choose Analysis to setup analysis. In the Analysis section, select tran, set stop time to 200ns, Click on the moderate and Enabled buttons at the bottom, and then click Apply.



DC Analysis

- DC ANALYSIS: In ADE window, Analysis-> Choose Analysis to setup analysis. In the Analysis section, select dc, turn on **Save DC Operating Point, t**urn on the **Component Parameter,** and Click the **Select Component**.

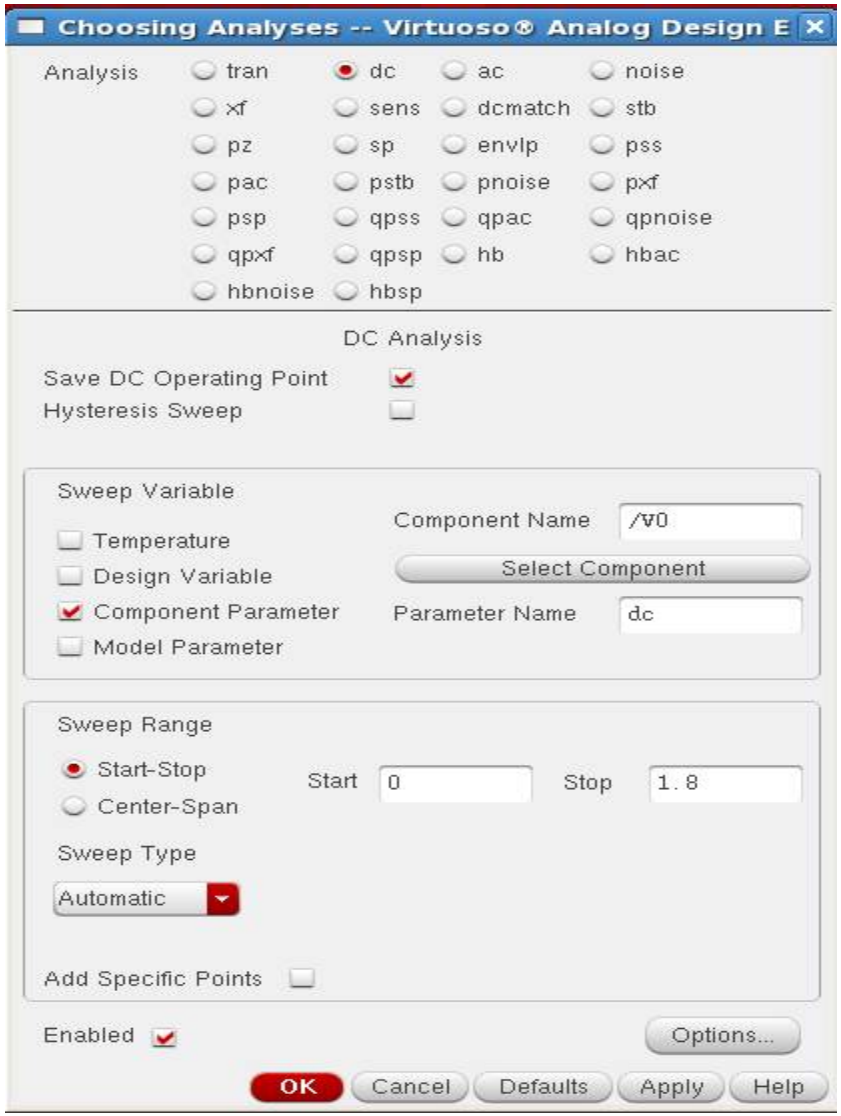




- Select input signal vpulse source in the test schematic window.
- Select DC Voltage in the “Select Component Parameter window and click OK.

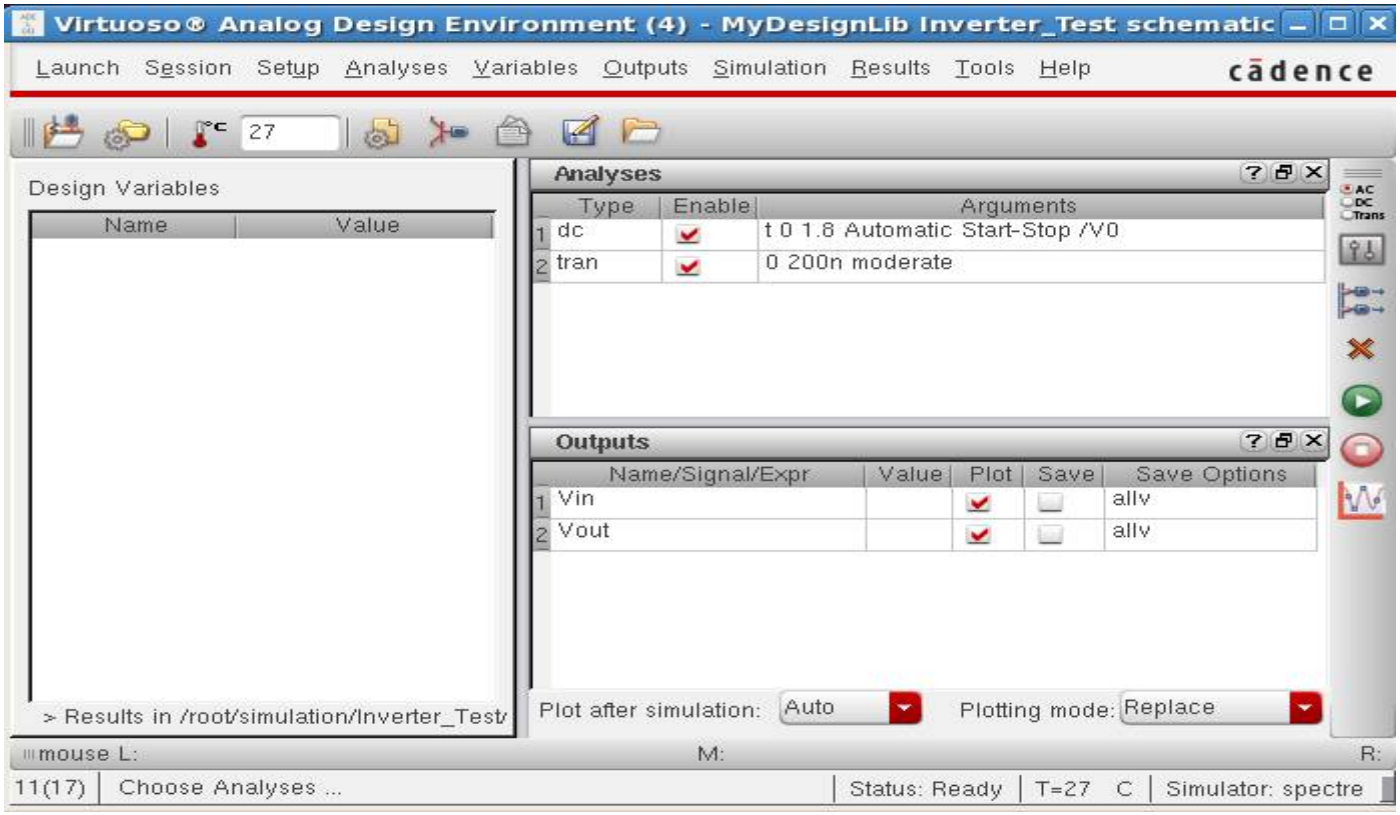
DC Analysis

- In the analysis form, enter start and stop voltages as 0 to 1.8 respectively.
- Check the enable button and then click Apply.
- Click OK in the Choosing Analysis Form.



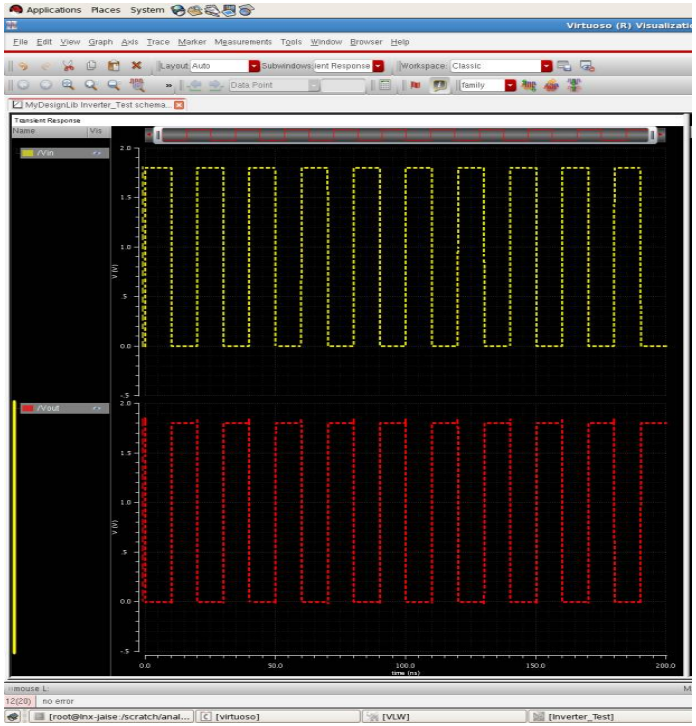
Setting Output Variables

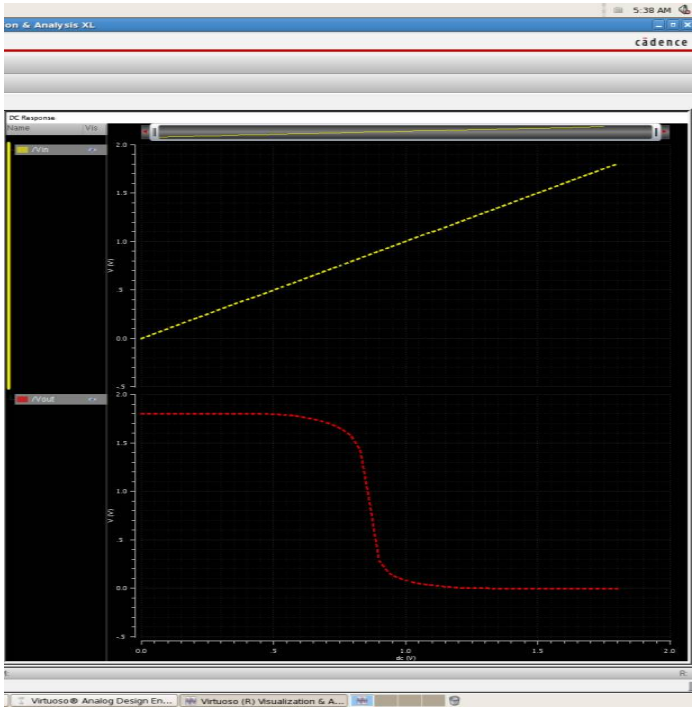
- SETTING OUTPUT VARIABLES: In ADE window, Outputs –> To be plotted –> Select on Schematic.
- After setting the transient and DC analysis and also the signals for wave plotting, the ADE L window will look like the figure below.



Running Simulation

- RUNNING SIMULATION: In ADE window, Simulation –> Netlist and Run or click 
- This will create the netlist as well as run the simulation.





- The above graphs depict the transient and DC analyses outputs. The DC analysis graph shows the output value for an input sweep range of 1 to 1.8V.

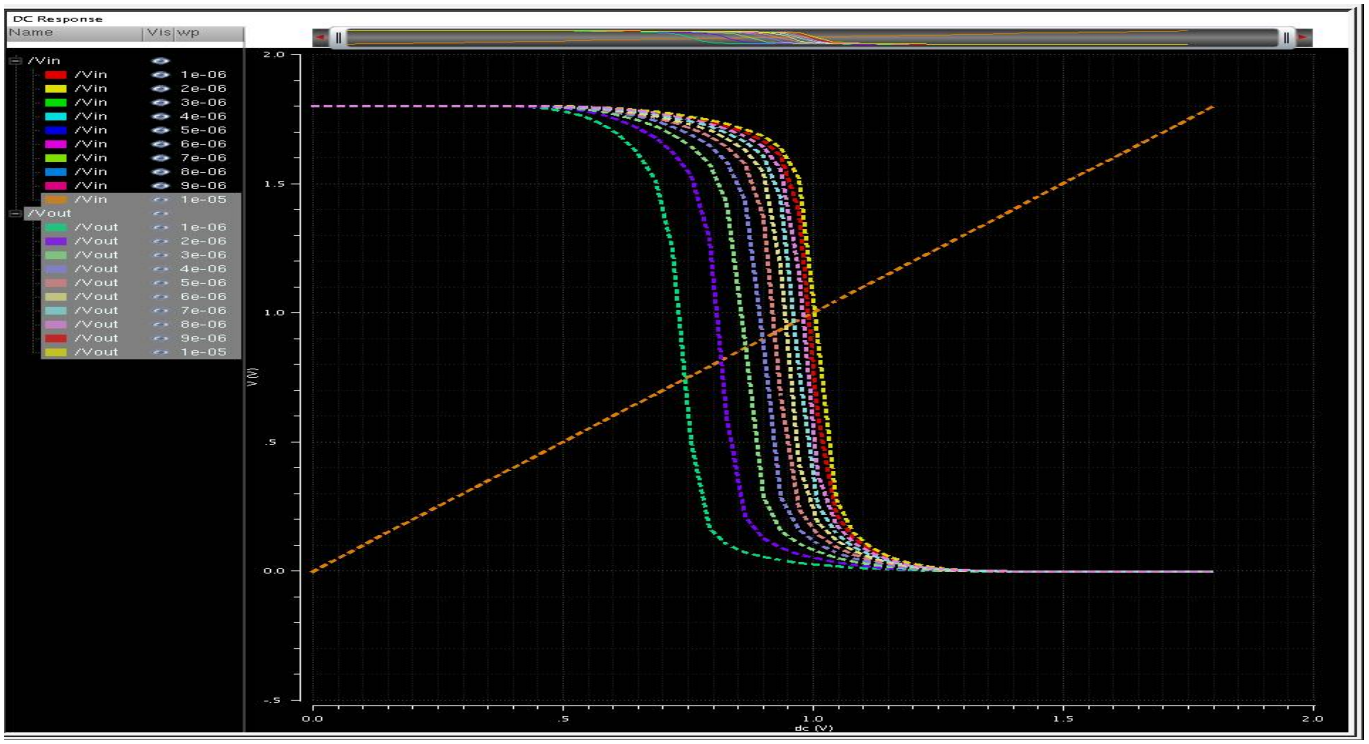
Parametric Analysis

- PARAMETRIC ANALYSIS: In the Simulation window, Tools—> Parametric Analysis. The Parametric Analysis form opens.
- In the Parametric Analysis window, double click on the Add Variable field to select the parameter. Change the Range Type, Step Mode and Total Steps fields in the Parametric Analysis form.

- Device Sizing: Size variation test help to determine the optimized transistor size. DC analysis on a inverter is carried out for testing the performance at various pull up transistor size

Parametric Analysis

- Analysis—>Start Selected or click  Run Selected Sweeps icon in the Parametric Analysis window.



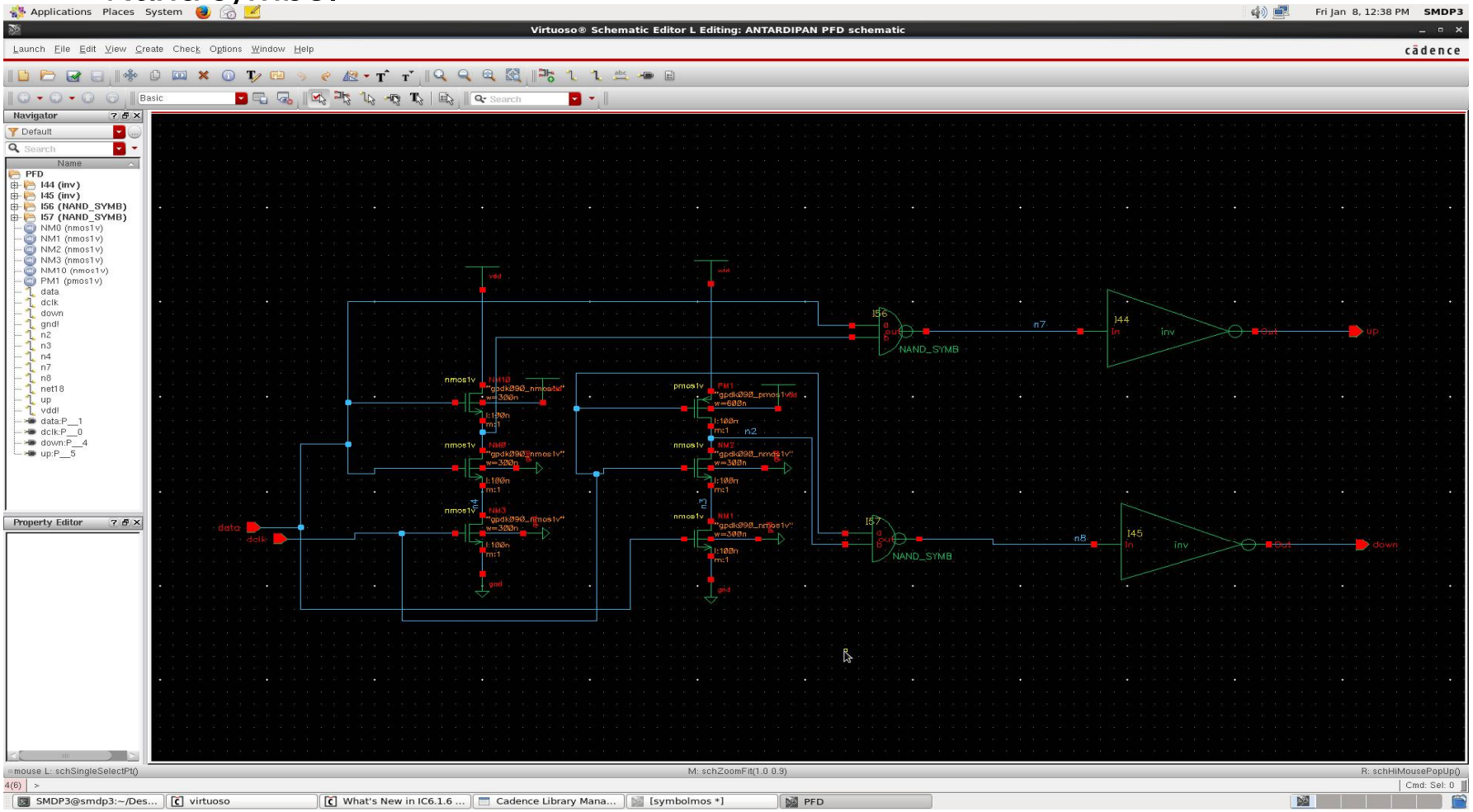
- Output waveform of Inverter at various pull-up transistor size.
- From this analysis the optimum device size for best result can be chosen.

Inherited designs

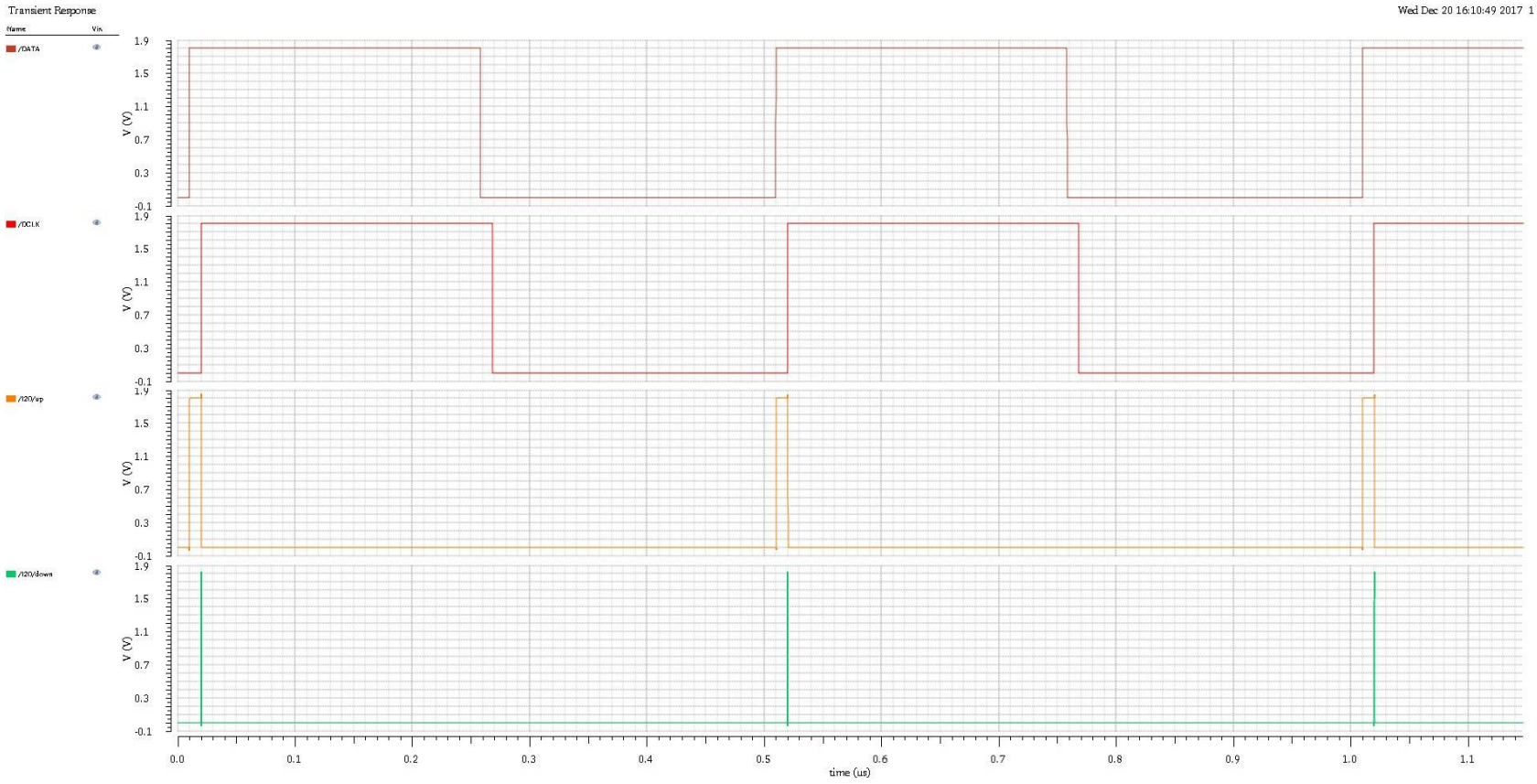
- Semi custom design approach is necessary for a short term project. Many optimised designs can be used with this new design line a controller or filter.
- Standard cells can also be used with core cells and the complete design can be fabricated successfully. The section below shows steps on designing a cell that uses both core cells and the earlier made designs.

Inherited designs

- PFD(Phase Frequency Detector) Schematic using pre-made Inverter & Nand symbol



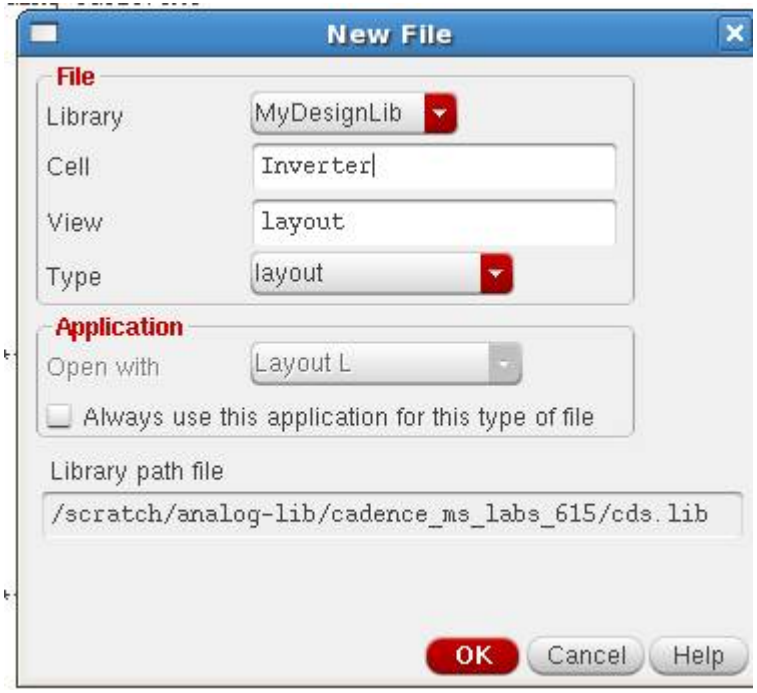
PFD Schematic Output



Output waveform of PFD

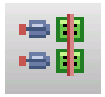
Creating Layout

- From the Inverter schematic window menu execute Launch – Layout XL. A “Startup Option” form appears
- Select Create New option and click OK



- A —New File‖ form appears, Check the Library (MyDesignLib), Cell name (Inverter) and View name (layout
- Click OK from the —New File‖ Window. LSW (Layer Select Window) and a blank layout window appear along with schematic window

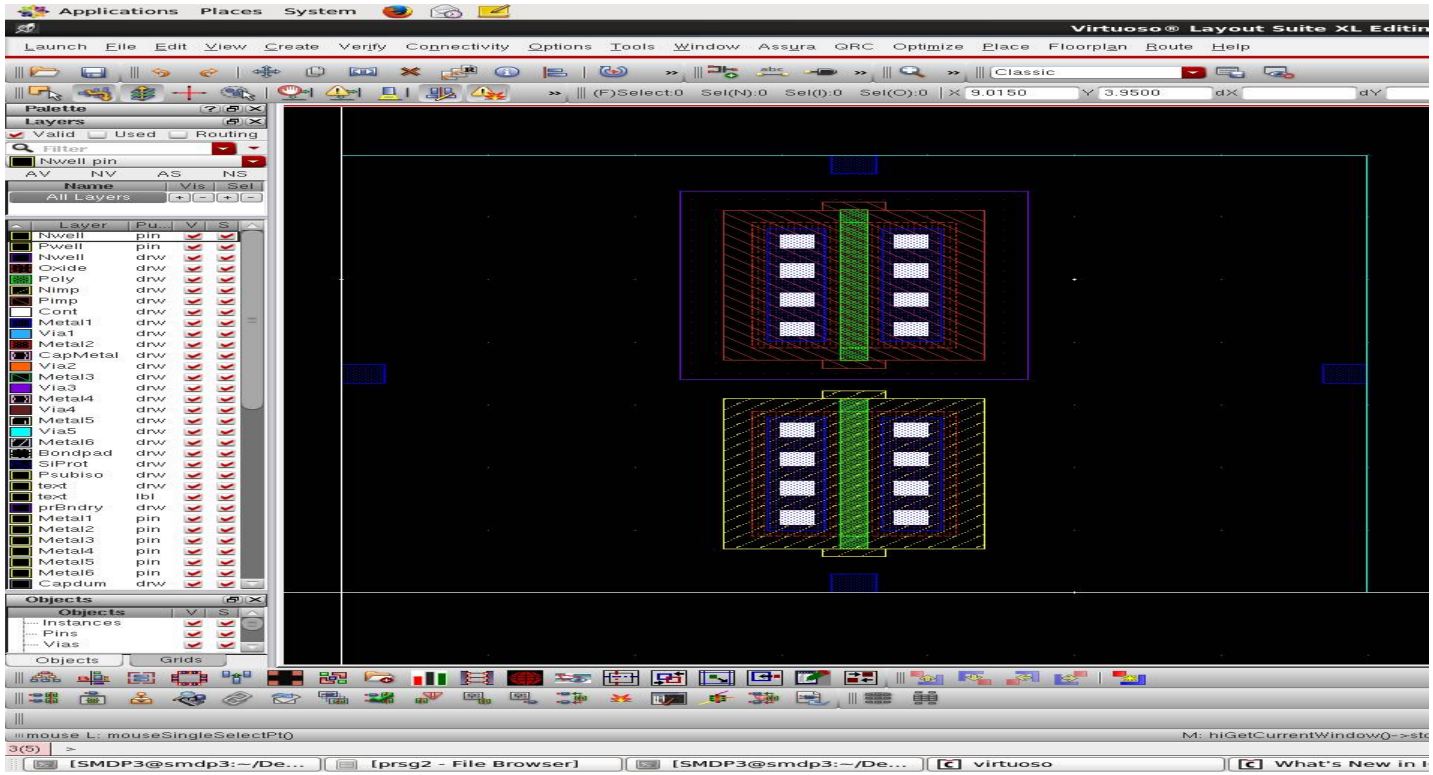
Adding Components to Layout

- Execute **Connectivity – Generate – All from Source or click the icon**  **in the —Layout Editor window", Generate Layout form appears. Click OK which imports the schematic components in to the Layout window automatically .**
- **The table provide bellow quick access keys and their function in the layout**

key	Function
Ctrl+Shift+W	Create wire
I	Insert Instance
Q	properties
ctrl+Z	Zoom in
Shift+Z	Zoom out
F	Fit to screen
Z	Zoom to Area
Ctrl+T	Zoom to selected
Del	Delete
S	Stretch
C	Copy
U	Undo
O	Create via
K	Create ruler

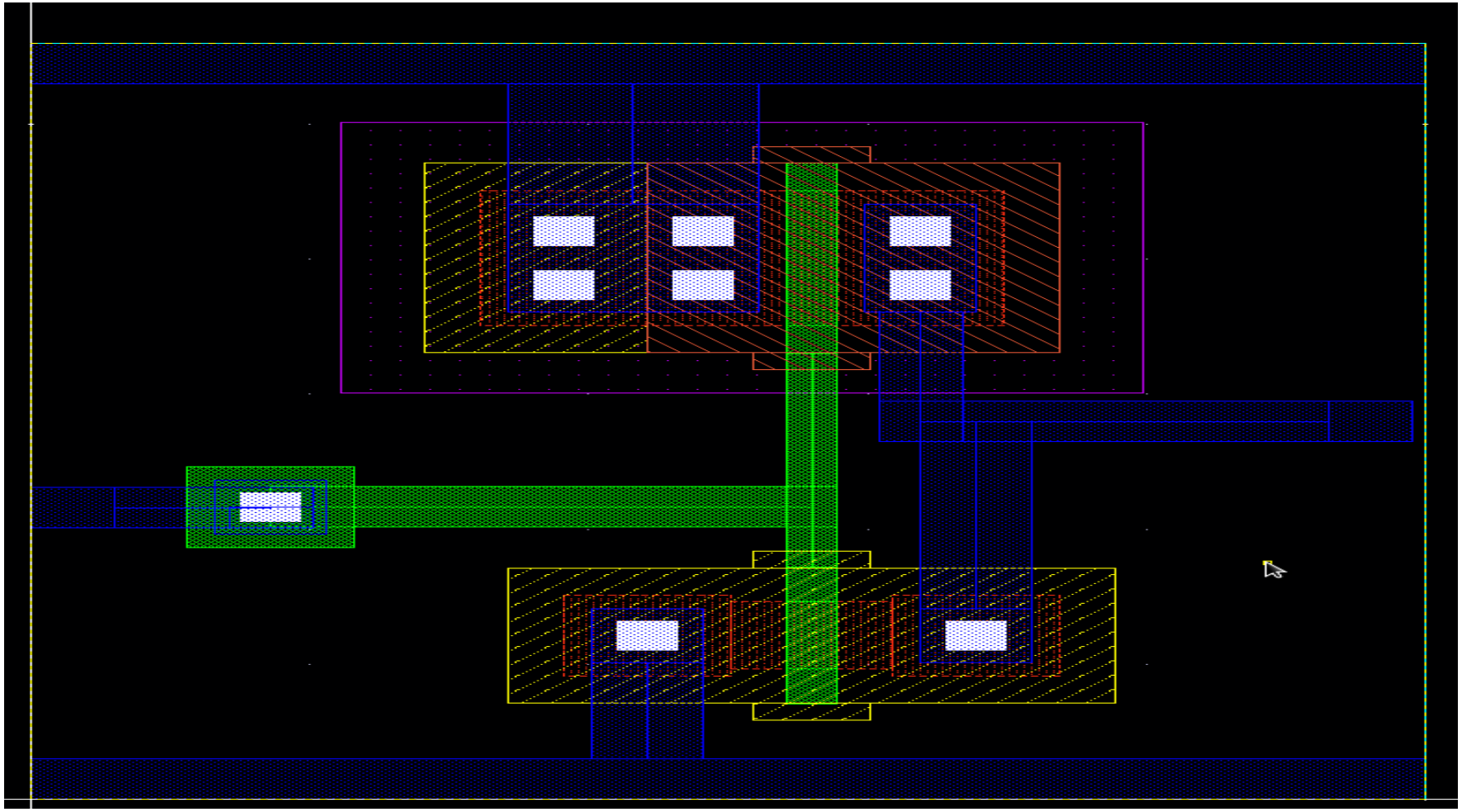
Layout

- move a device to get the connectivity information, which shows the guide lines (or flight lines) for the inter connections of the components.
- From the layout window execute **Create – Shape – Path or Create wire or click or Create – Shape – Rectangle (for vdd and gnd bar) and select the appropriate Layers from the LSW window and Vias for making the inter connections**
- We will use the contacts or vias to make connections between two different layers



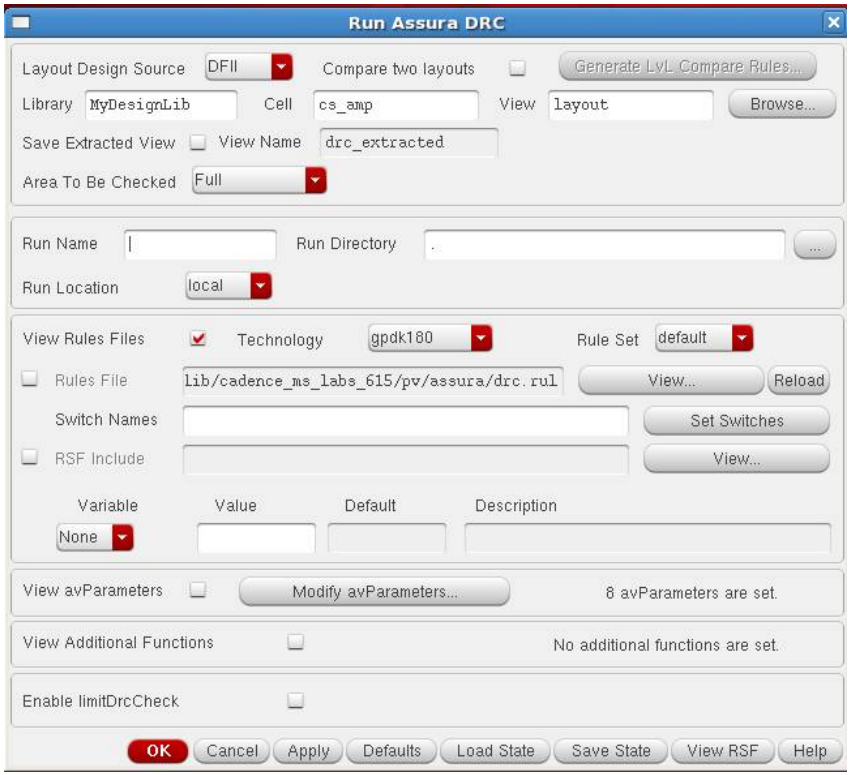
Saving the Layout design

- Final Inverter layout should appear as below

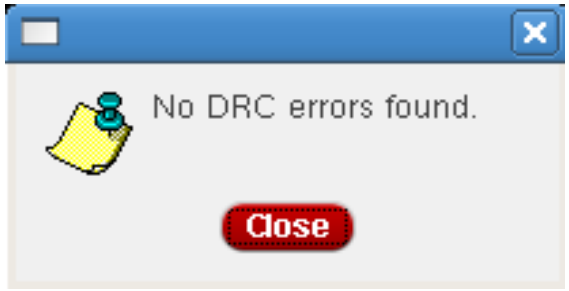


Physical Verification

- Here we check whether our design obeys the design rules
- **Running a DRC:** Select **Assura - Run DRC from layout window. The DRC form appears. The Library and Cell name are taken from the current design window, but rule file may be missing. Select the Technology as gpdk180*. This automatically loads the rule file***



When DRC finishes, If there are no errors in the layout then a dialog box appears with **No DRC errors found written in it, click on close to terminate the DRC run**

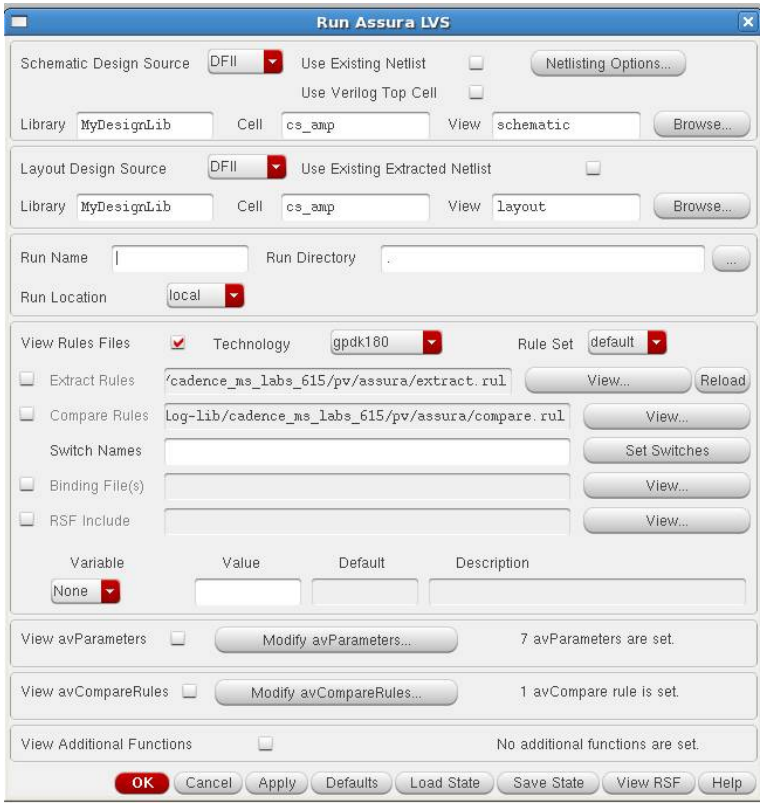


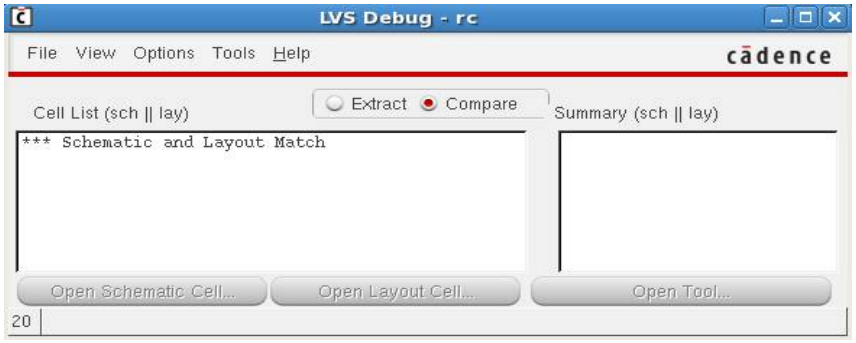
Assura LVS

- In this section we will perform the LVS check that will compare the schematic netlist and the layout netlist
- **Running LVS:** Select **Assura – Run LVS from the layout window. The —"Run Assura LVS" form appears. It will automatically load both the schematic and layout view of the cell**

Once the LVS is completed, a window informs that the LVS completed successfully and asks if you want to see the results of this run. Click **Yes in the window.**

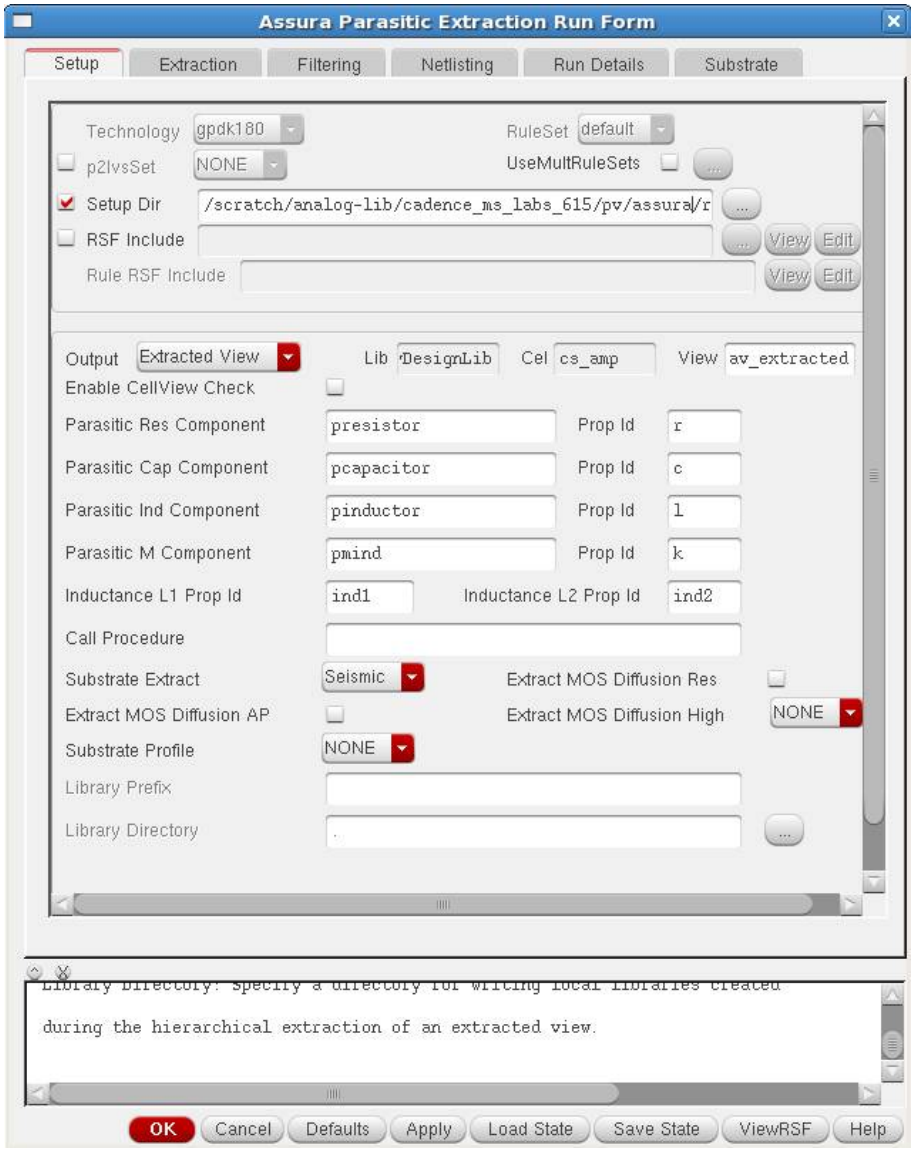
If the schematic and layout matches completely, you will get a window displaying **Schematic and Layout Match. Close the window to terminate the LVS run**





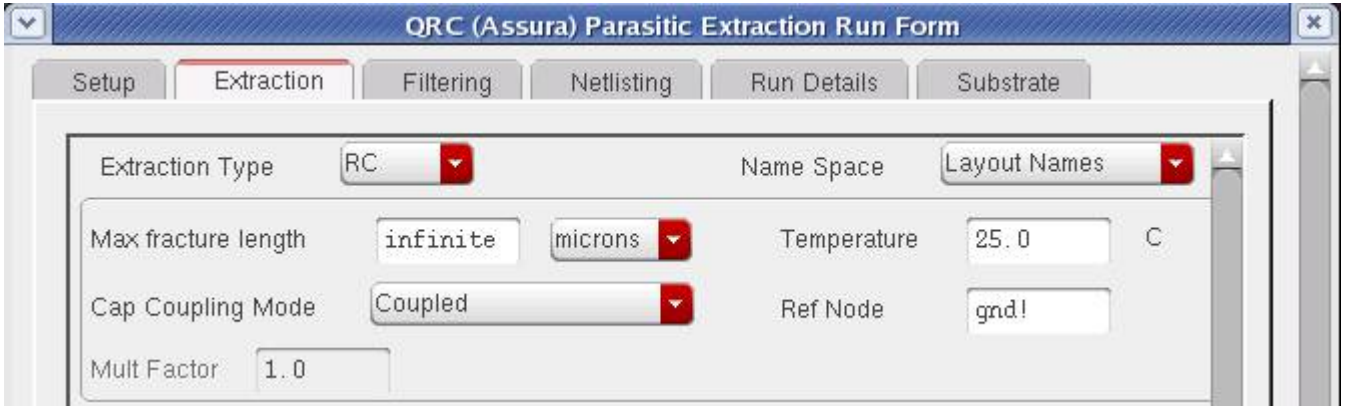
Assura RCX

- In this section we will extract the RC values from the layout and perform analog circuit simulation on the designs extracted with RCX. Before using RCX to extract parasitic devices for simulation, the layout should match with schematic completely to ensure that all parasites will be backannoted to the correct schematic nets.
- **Running RCX:** From the layout window execute **Assura – Run RCX**
- Change the following in the "**Assura parasitic extraction run form||. Select Output type under Setup tab as Extracted View.**



Parasitic Extraction

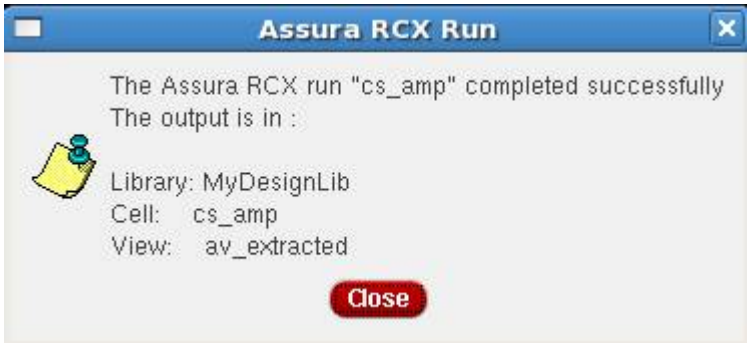
- In the **Extraction tab of the form, choose Extraction type, Cap Coupling Mode and specify the Reference node for extraction.**



In the **Filtering tab of the form, Enter Power Nets as vdd!, vss! and Enter Ground Nets as gnd!**

av_extracted

- When RCX completes, a dialog box appears, informs you that **Assura RCX run Completed successfully. Click on close to terminate the RCX run.**

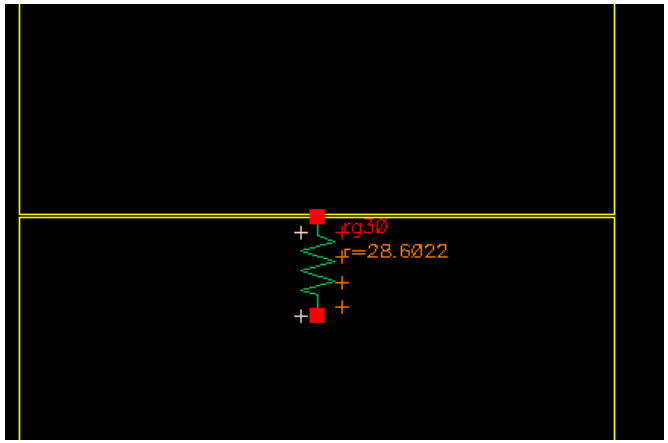


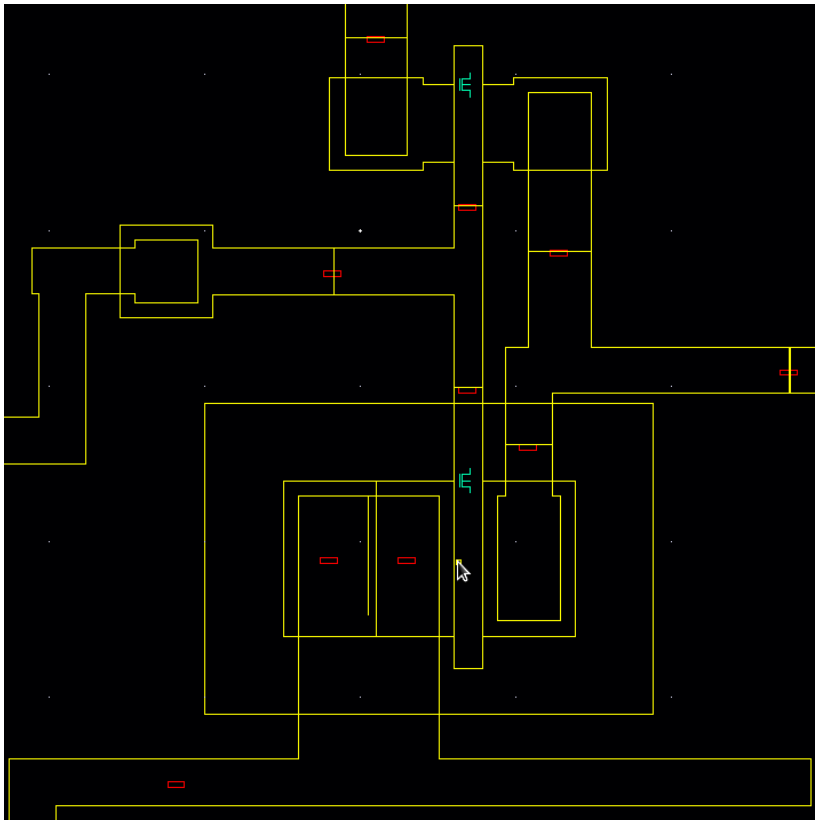
Configuring Layout

- The layout must be configure before being put on test. The layout once corrected from all the design rule errors, a LVS test is performed for the cell. The chance of getting the error become minimum when the layout is generated from the connectivity window. The parasitic extraction is carried out next and the excreted layout is saved for the testing purpose.

Fig. shown av_extracted view of the layout

Press **shift-f to view values of the extracted resistance and capacitance in the av_extracted view**

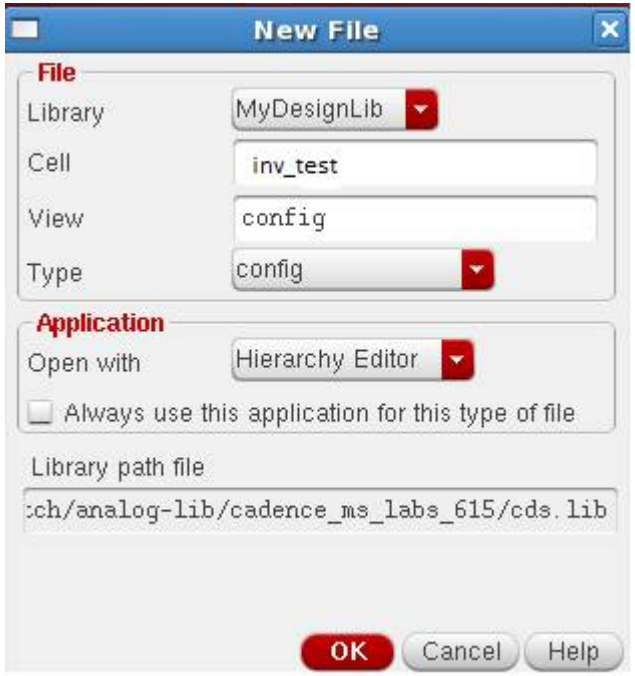


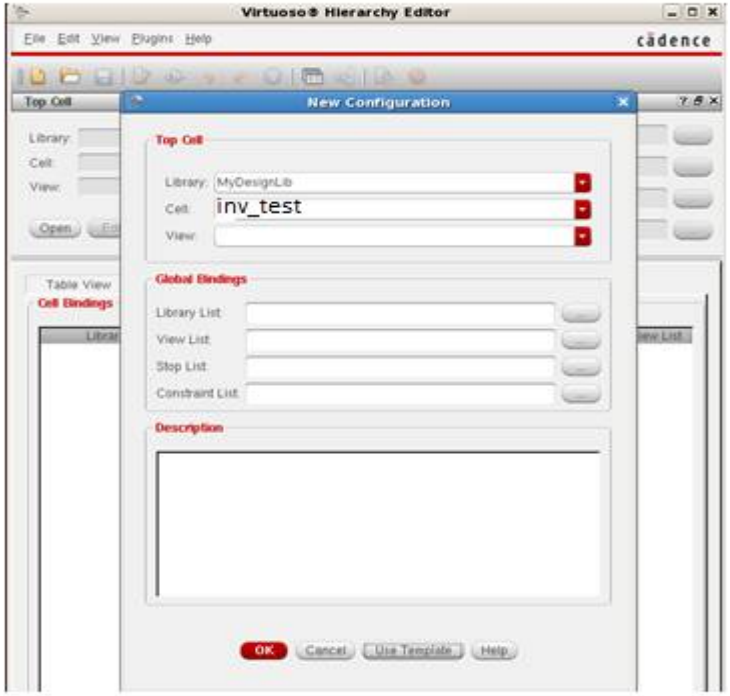


Creating the Configuration View

- In the CIW or Library Manager, execute **File – New – Cell view**
- In the Create New file form, set the following:

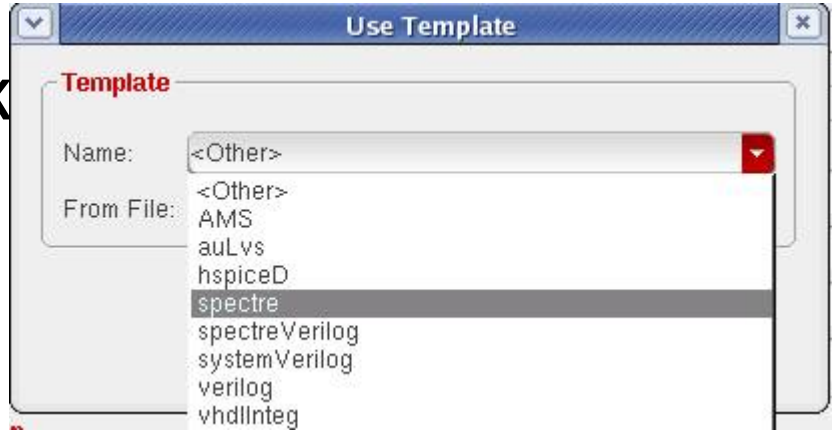
  Click **OK in "New File" form. The "Hierarchy Editor" form opens and a "New Configuration" form opens in front of it.**

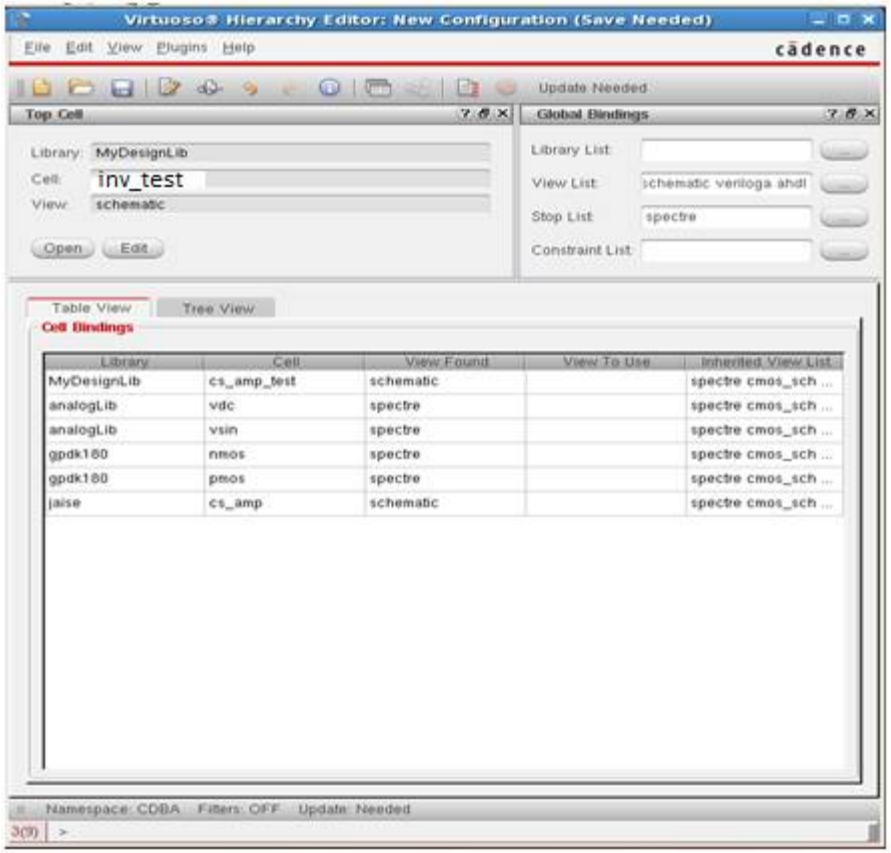




Creating the Configuration View

- Click **Use template at the bottom of the New Configuration form and select Spectre in the cyclic field and click OK**





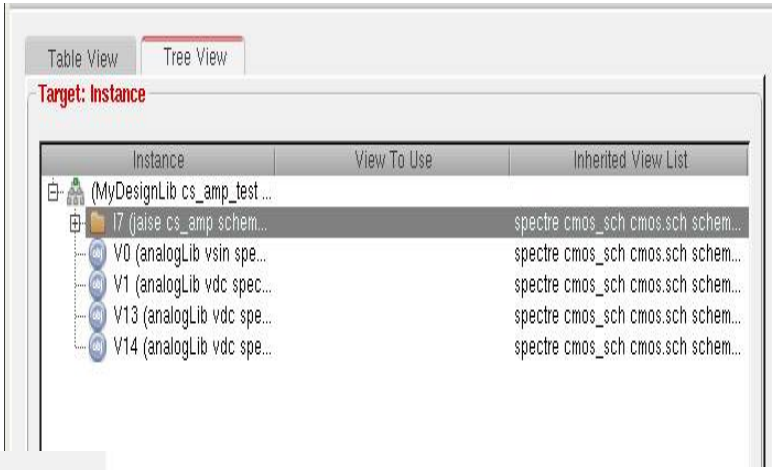
Change the **Top Cell - View to schematic and remove the default entry from the Library List field and Click OK in the New Configuration form.**

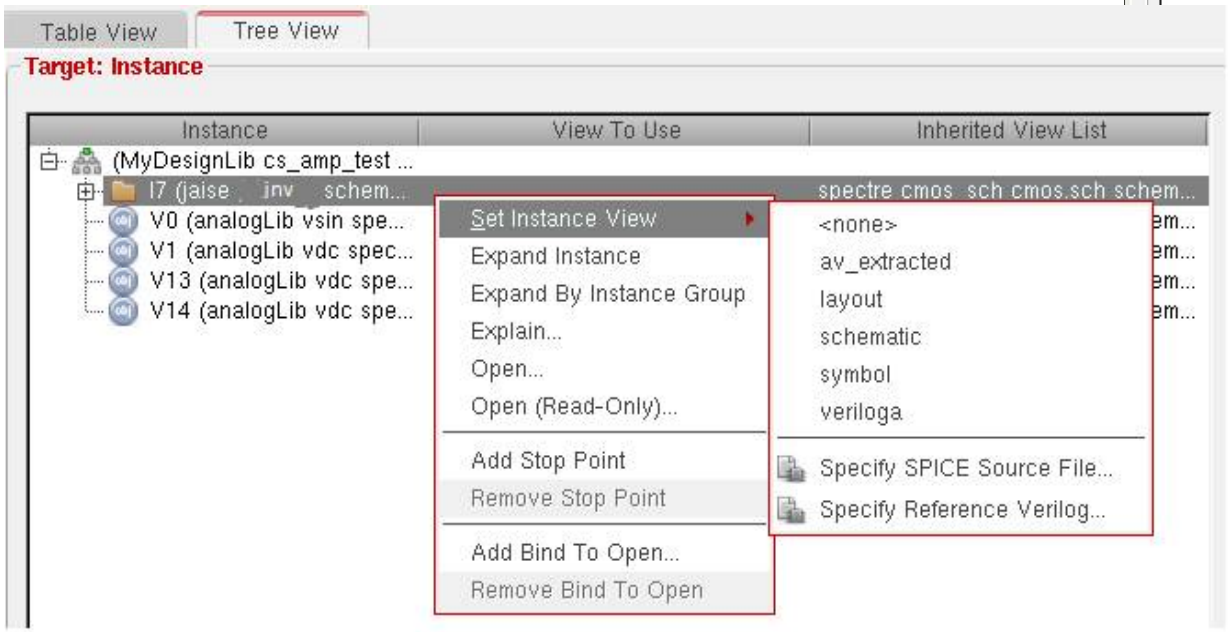
The hierarchy editor displays the hierarchy for this design using table format

Creating the Configuration View

- Click the **Tree View tab. The design hierarchy changes to tree format. The form should look like this**

  Choose the **inv** schematic folder icon and right click, a set of option arises, click on Set Instance View and choose av_extracted





Save the current configuration and Close the Hierarchy Editor window. Execute File – Close Window.

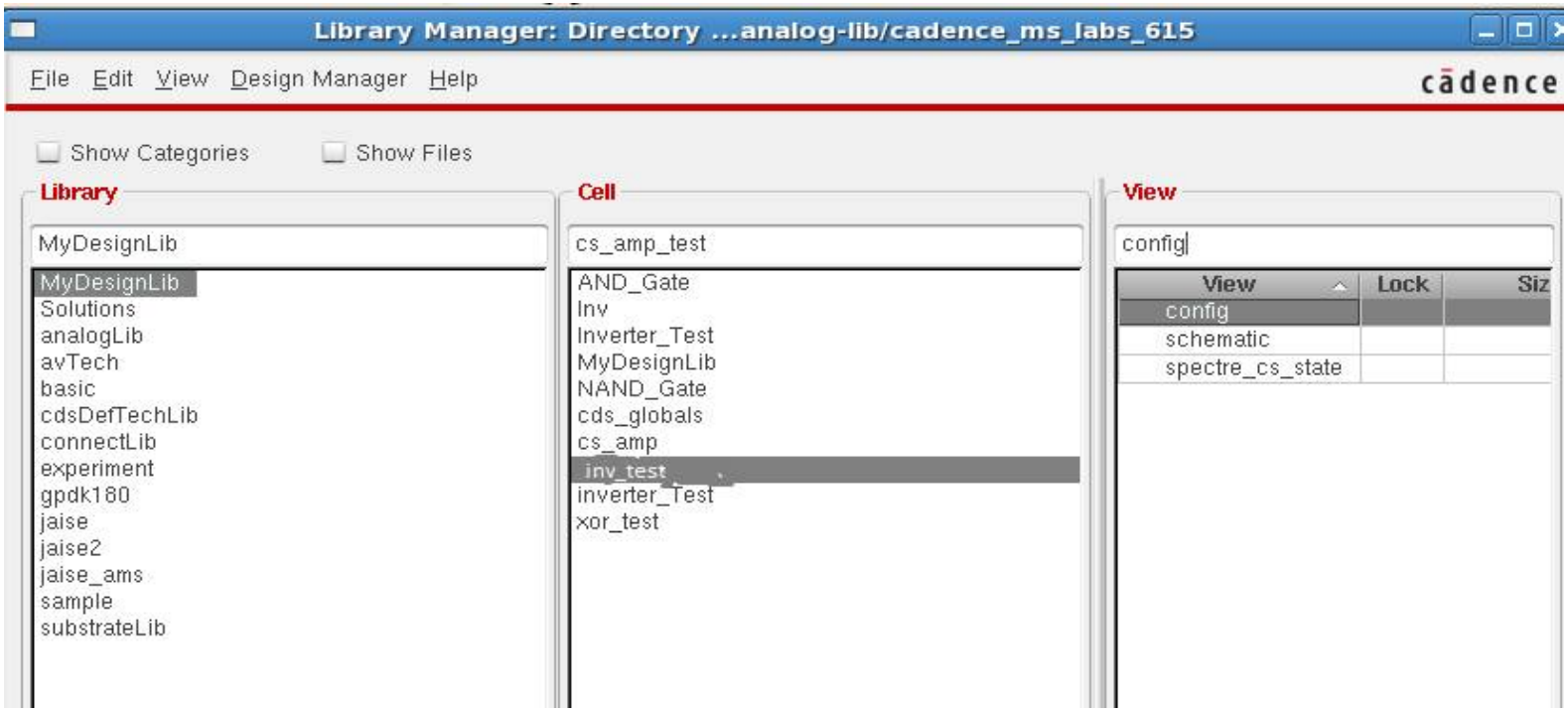
Post layout simulation

- In the library Manager window, select the following

  Library ⟶ MyDesignLib

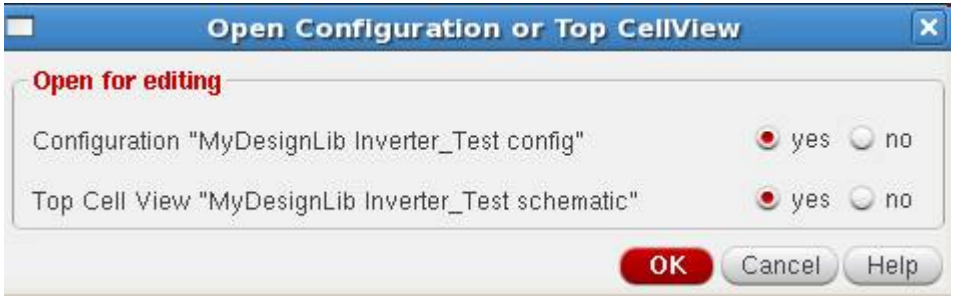
  Cell ⟶ Inv_test

- Double click on config under View



Post layout simulation

- A new —Open Configuration or Top CellView‖ form appears. Choose yes in both the cyclic fields and click OK



Simulation of config view with Spectre

- Execute Launch – ADE L from the schematic window
- follow the same procedure for running the simulation
- Click Netlist and Run icon to start the simulation
- The simulation takes a few seconds and then waveform window appears

Design notes

- Use array structure for initial routing(horizontal 1/2 metal layers, Vertical 1/2 metal layer)
- Avoid longer routing (often suffer from charg coupling and slower)
- The layout design can be optimized in the schematic design (proper cell placement)
- Pin placement of sub-circuits is extremely important in large design
- Avoid excess via creation(current conduction is poor in Vias)

Thank you