SPICE modeling

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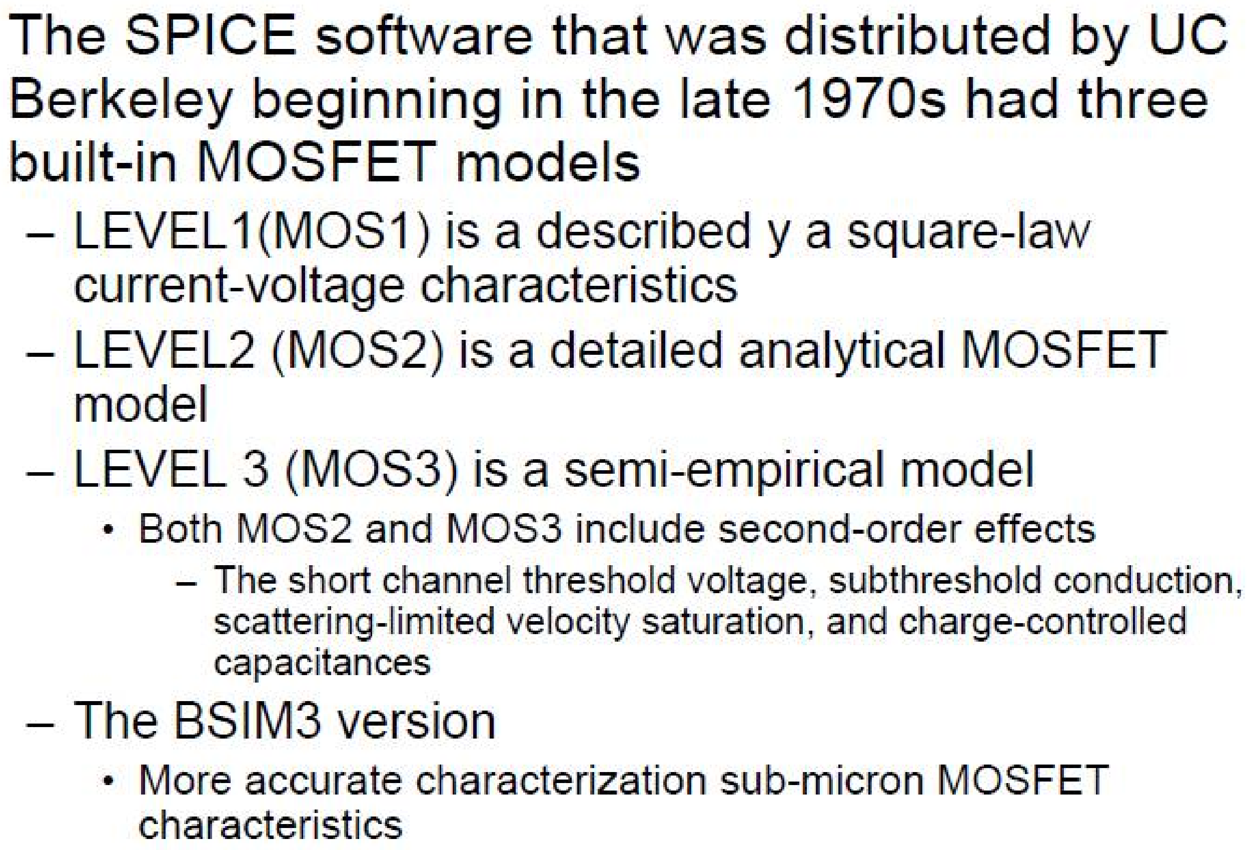
Introduction

- **SPICE** (*Simulation Program with Integrated Circuit Emphasis*) is a general-purpose, open source analog electronic circuit simulator. It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior. It is used in transistor level design.



The SPICE software that was distributed by UC Berkeley beginning in the late 1970s had three built-in MOSFET models

- LEVEL1(MOS1) is a described y a square-law current-voltage characteristics
- LEVEL2 (MOS2) is a detailed analytical MOSFET model
- LEVEL 3 (MOS3) is a semi-empirical model
  - Both MOS2 and MOS3 include second-order effects
    - The short channel threshold voltage, subthreshold conduction, scattering-limited velocity saturation, and charge-controlled capacitances
- The BSIM3 version
  - More accurate characterization sub-micron MOSFET characteristics

1. First Generation Models (Level 1, Level 2, Level 3 models)
2. Second Generation Models (BISM, BSIM2, HSPICE Level 28)
3. Third Generation Models (Level 7, Level 48, BSIM3, etc.)

- **Level 1:**

  -developed in 1973

  -was originally written in FORTRAN.

  -Though rarely used can be used for quick estimates when accuracy is not a concern.

  -It used nodal analysis and fixed step transient analysis which were creating problems and hence an improved version called SPICE level 2 came into picture.

- **Level 2:**

  -was released 2 years later

  -was written in FORTRAN as well.

  -was capable of doing many things like AC analysis, DC analysis, noise analysis , DC transfer curve analysis, Transfer function analysis, Transient analysis.

  -Analysis at various temperatures was done by automatically updating semiconductor model parameters for temperature, allowing the circuit to be simulated at temperature extremes.

- **Level 3:**
  - -was released in 1989.
  - -was written in C.
  - -more sophisticated MOSFET models.
  - -it had a command line feature.

BSIM:

- Commercial and industrial SPICE simulators have added many other device models as technology advanced and earlier models became inadequate.
- To attempt standardization of these models so that a set of model parameters may be used in different simulators, an industry working group was formed, called the Compact Model Council to choose, maintain and promote the use of standard models. The BSIM family of models are some of the standard models .HSpice ,Spectra etc. are based on these.

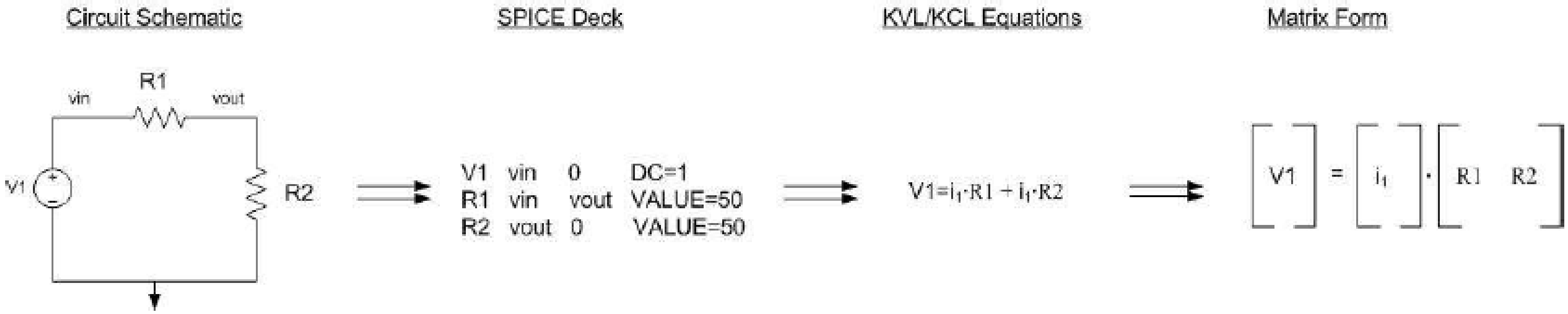
Adoptions:

- LTSpice owned by Linear technologies
- TINA owned by TI.
- HSpice owned by Synopsys.
- Power spice owned by IBM.
- TITAN by Infineon.
- MultiSim by National Instruments.

How does SPICE work?

For a given circuit, KCL and KVL equations can be written and these equations can be solved using Matrix math

SPICE does the same thing, except on the front-end it is able to take the entered circuit and create the KCL/KVL equations for us



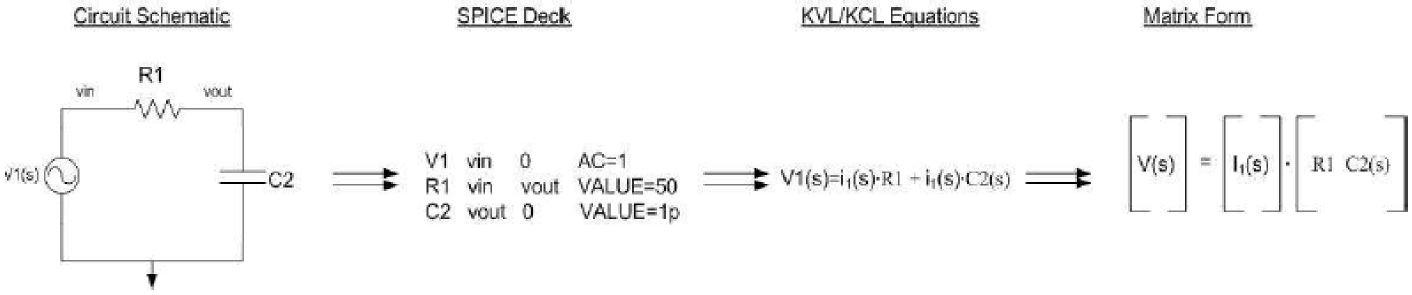
Circuit Schematic ⇒ SPICE Deck ⇒ KVL/KCL Equations ⇒ Matrix Form

```
V1  vin   0     DC=1
R1  vin   vout  VALUE=50
R2  vout  0     VALUE=50
```

$$V1=i_1 \cdot R1 + i_1 \cdot R2$$

$$\begin{bmatrix} V1 \end{bmatrix} = \begin{bmatrix} i_1 \end{bmatrix} \cdot \begin{bmatrix} R1 & R2 \end{bmatrix}$$

This can also be extended to AC analysis since the matrix math can handle Complex numbers



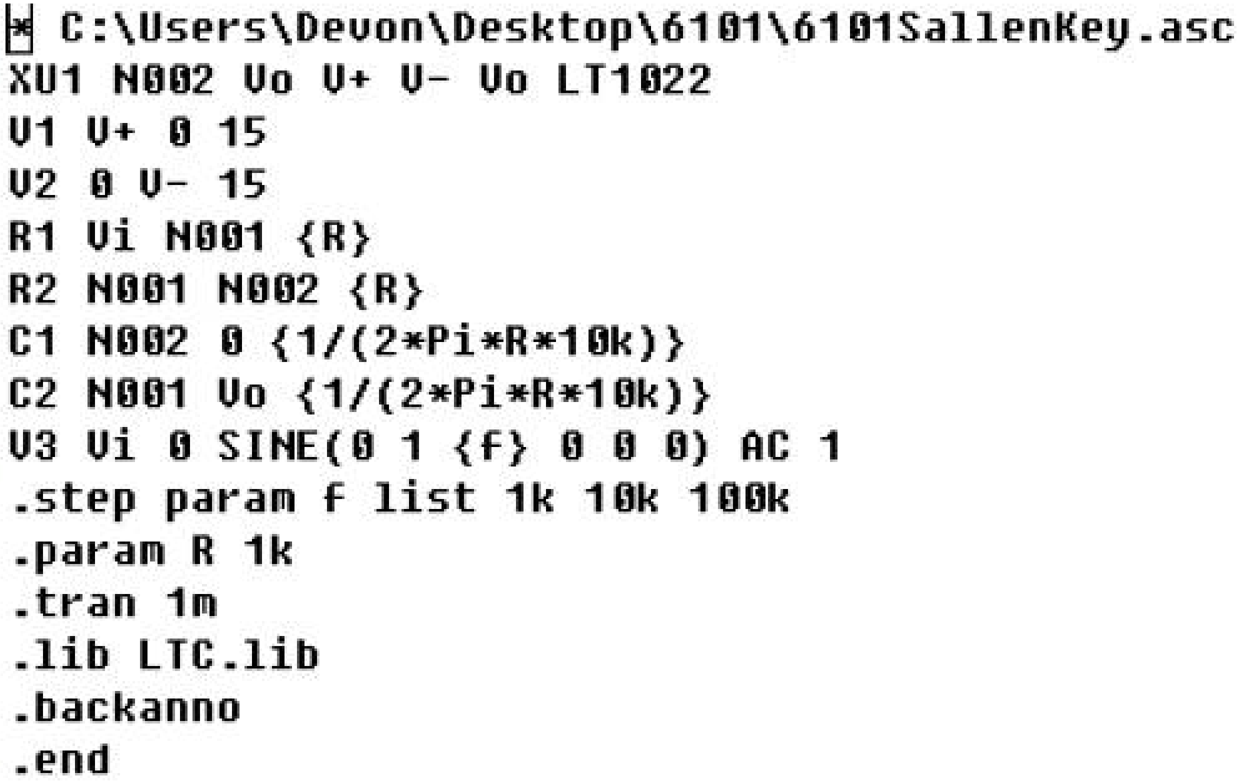
Circuit Schematic ⇒ SPICE Deck ⇒ KVL/KCL Equations ⇒ Matrix Form

```
V1  vin   0     AC=1
R1  vin   vout  VALUE=50
C2  vout  0     VALUE=1p
```

$$V1(s)=i_1(s) \cdot R1 + i_1(s) \cdot C2(s)$$

$$\begin{bmatrix} V(s) \end{bmatrix} = \begin{bmatrix} I_1(s) \end{bmatrix} \cdot \begin{bmatrix} R1 & C2(s) \end{bmatrix}$$

Netlists

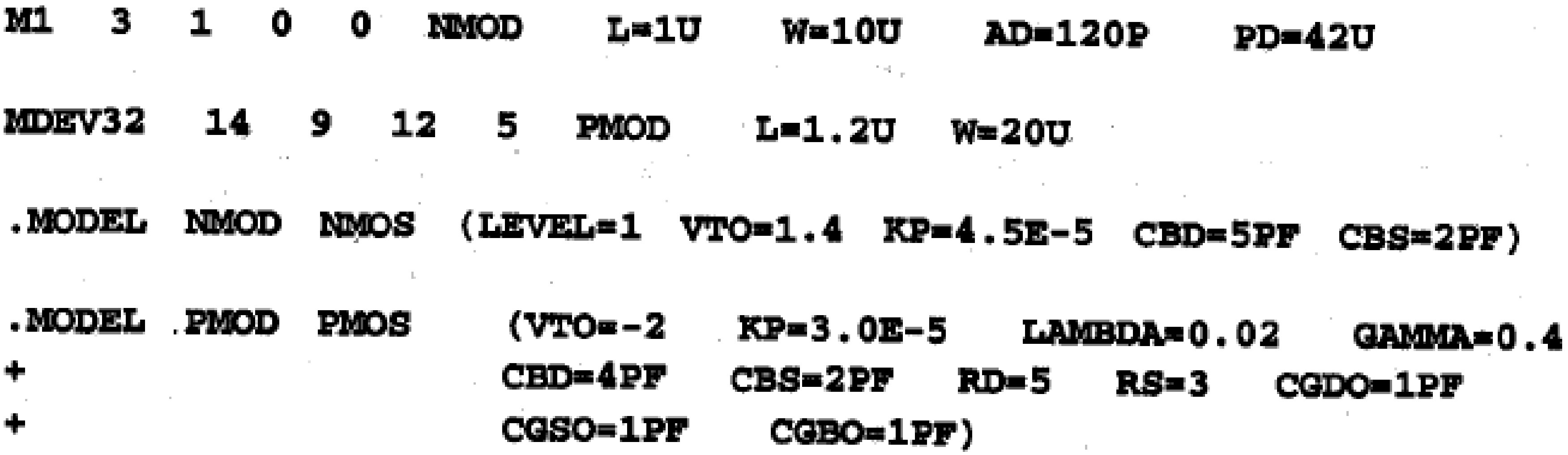


```
* C:\Users\Devon\Desktop\6101\6101SallenKey.asc
XU1 N002 Vo V+ V- Vo LT1022
V1 V+ 0 15
V2 0 V- 15
R1 Vi N001 {R}
R2 N001 N002 {R}
C1 N002 0 {1/(2*Pi*R*10k)}
C2 N001 Vo {1/(2*Pi*R*10k)}
V3 Vi 0 SINE(0 1 {f} 0 0 0) AC 1
.step param f list 1k 10k 100k
.param R 1k
.tran 1m
.lib LTC.lib
.backanno
.end
```

Components

Commands

.MODEL for active device modeling



```
M1     3   1   0   0   NMOD    L=1U    W=10U    AD=120P    PD=42U

MDEV32   14   9   12   5   PMOD    L=1.2U   W=20U

.MODEL  NMOD  NMOS  (LEVEL=1  VTO=1.4  KP=4.5E-5  CBD=5PF  CBS=2PF)

.MODEL  PMOD  PMOS    (VTO=-2    KP=3.0E-5    LAMBDA=0.02    GAMMA=0.4
+                     CBD=4PF    CBS=2PF    RD=5    RS=3    CGDO=1PF
+                     CGSO=1PF    CGBO=1PF)
```

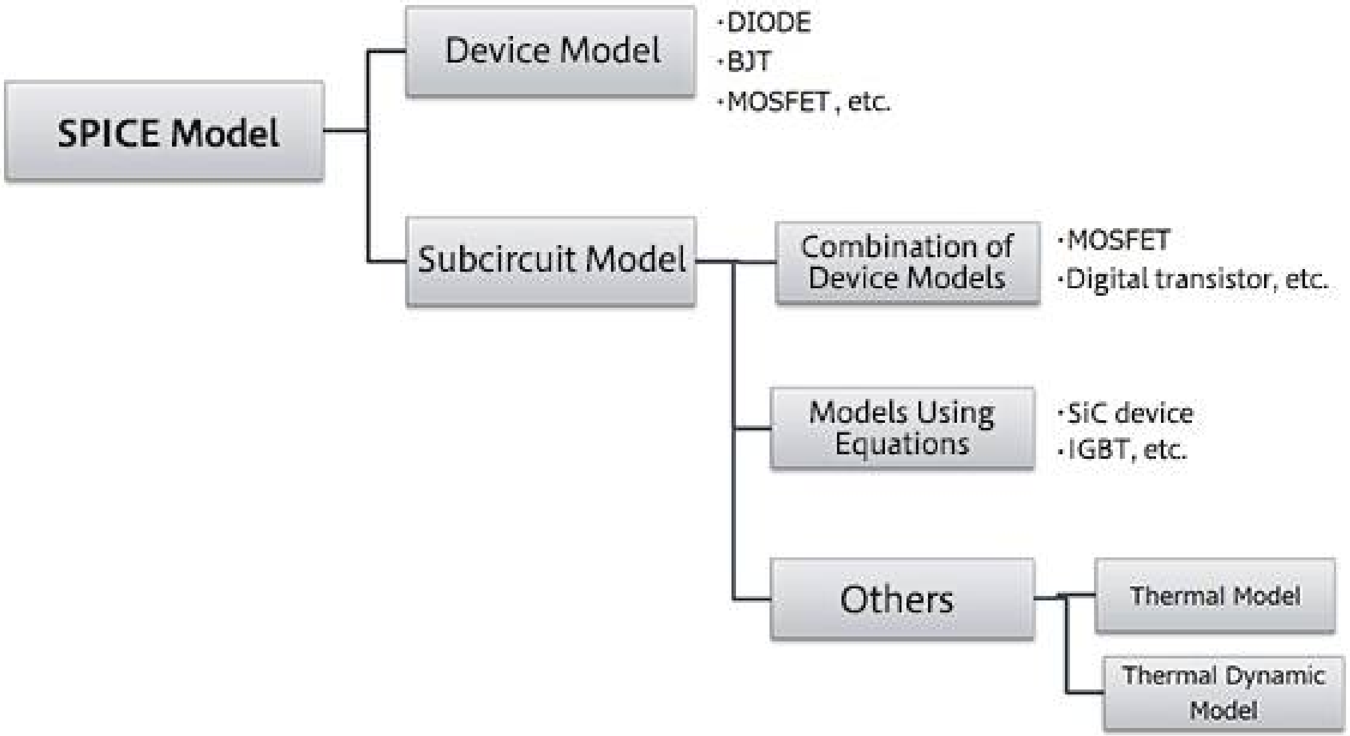
Types of Third-Party SPICE models

There are two types of third-party SPICE models:

- .MODEL: For intrinsic SPICE devices like diodes and transistors.
  - The .MODEL statement gives the parameters for the specific component.
  - The behavior of the device it intrinsically understood by SPICE, only the parameters need to be given to finish specifying the component's electrical characteristics.
- .SUBCKT: Define the modeled component by a collection of circuitry of intrinsic SPICE devices.
  - Example: an opamp would be modeled as a subcircuit.

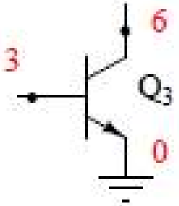
```
TITLE
ELEMENT DESCRIPTIONS
.MODEL STATEMENTS
ANALYSIS COMMANDS
OUTPUT COMMANDS
.END
```

```
Q<name> <nc> <nb> <ne> <model-name>
```



Device models essentially are models of elements such as diodes and MOSFETs. Subcircuit models are in essence combinations of device models, and can be thought of simply as circuit state models. In addition, there are also special models used to perform thermal calculations for circuits.

`Q3 6 3 0 my-npn` corresponds to

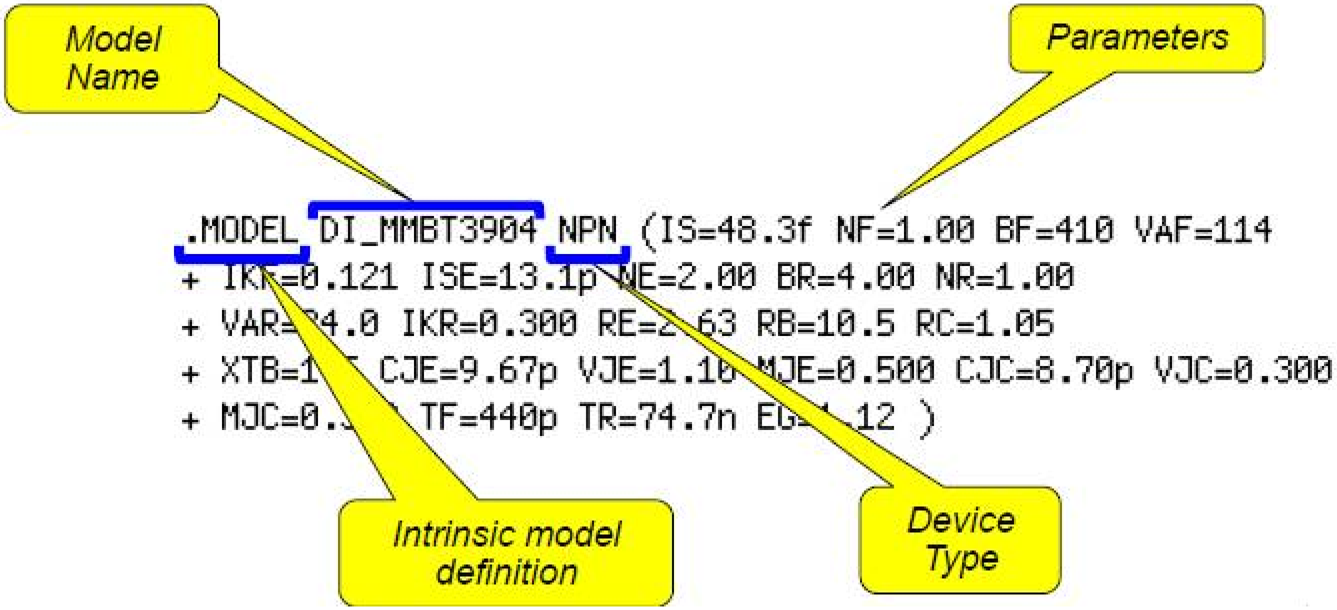


The `model-name` is defined as

```
.MODEL <model-name> <npn | pnp> ( [parameter = value] ...)
```

The syntax of an intrinsic model is:

.model *`<modelname>`* *`<DeviceType>`* *(`<parameter list>`)*



```
.MODEL DI_MMBT3904 NPN (IS=48.3f NF=1.00 BF=410 VAF=114
+ IKF=0.121 ISE=13.1p NE=2.00 BR=4.00 NR=1.00
+ VAR=24.0 IKR=0.300 RE=2.63 RB=10.5 RC=1.05
+ XTB=1.5 CJE=9.67p VJE=1.10 MJE=0.500 CJC=8.70p VJC=0.300
+ MJC=0.[illegible] TF=440p TR=74.7n EG=1.12 )
```

Importing Third-Party Intrinsic Models

To import a third-party intrinsic spice model

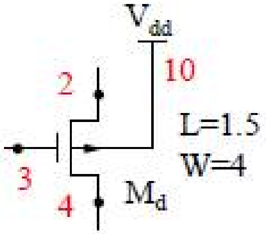
1.) Download the spice model file from the manufacturer's website. Make sure to note the file location on the hard-drive.

2.) Add the following spice directive to the LTspice simulation file (Edit pull-down menu ---> SPICE Directive):

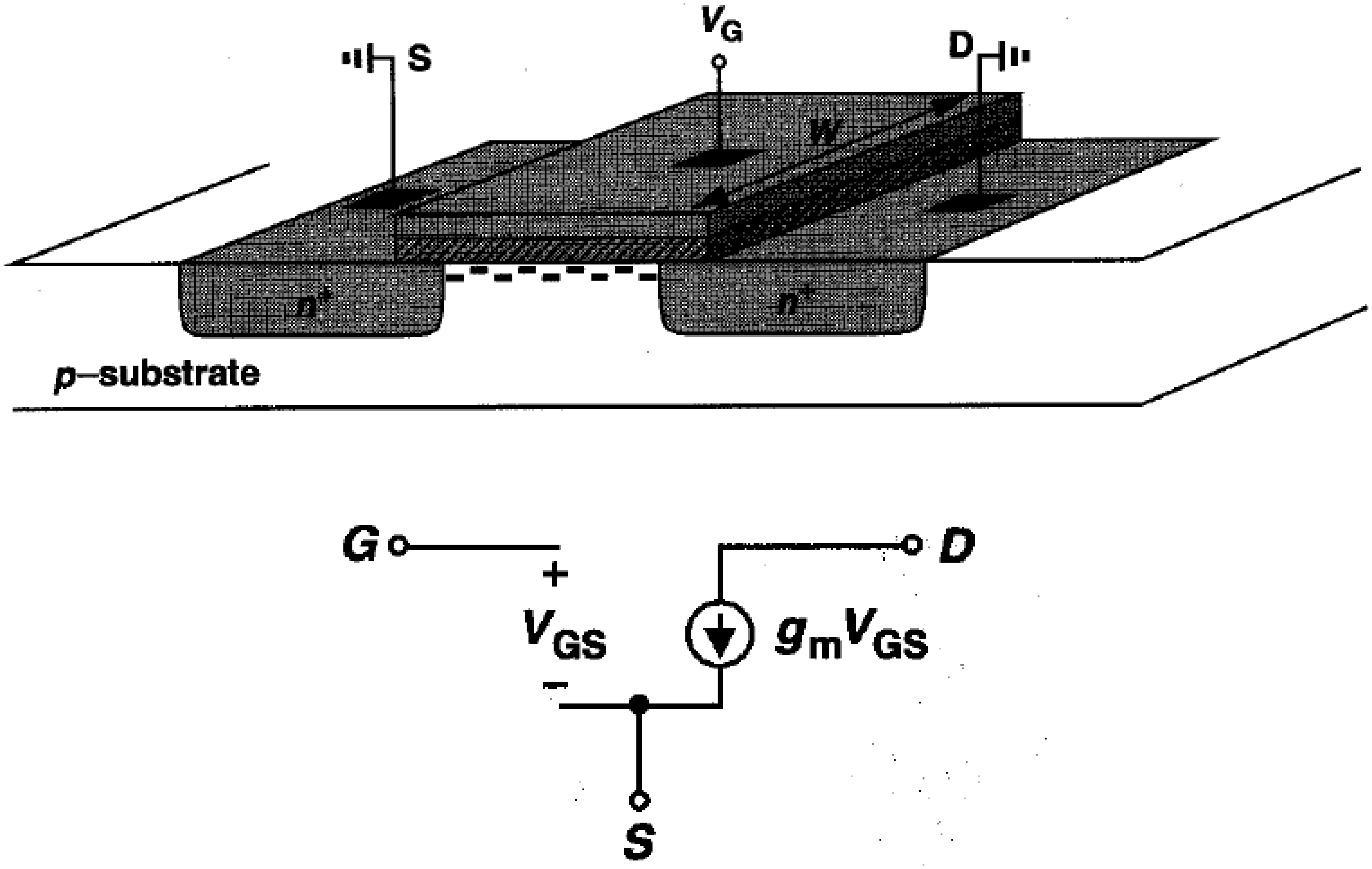
.include(1) *[*`path (optional)`*] spicemodel_filename.abc*

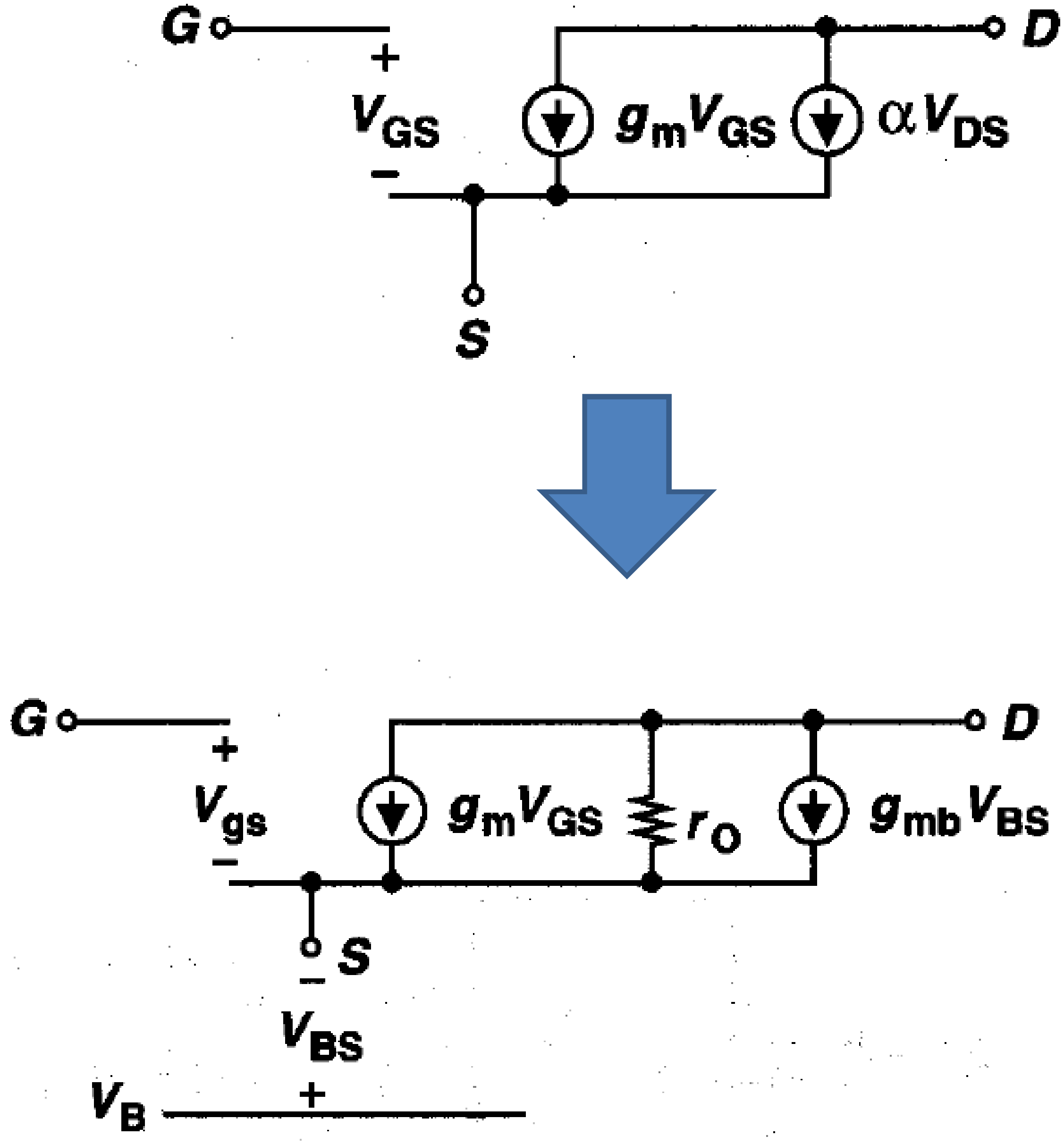
```
M<name> <nd> <ng> <ns> <nb> <model-name> [L=value] [W=value]
```

`Md 4 3 2 10 my-pmos L=1.5u W=4u` corresponds to

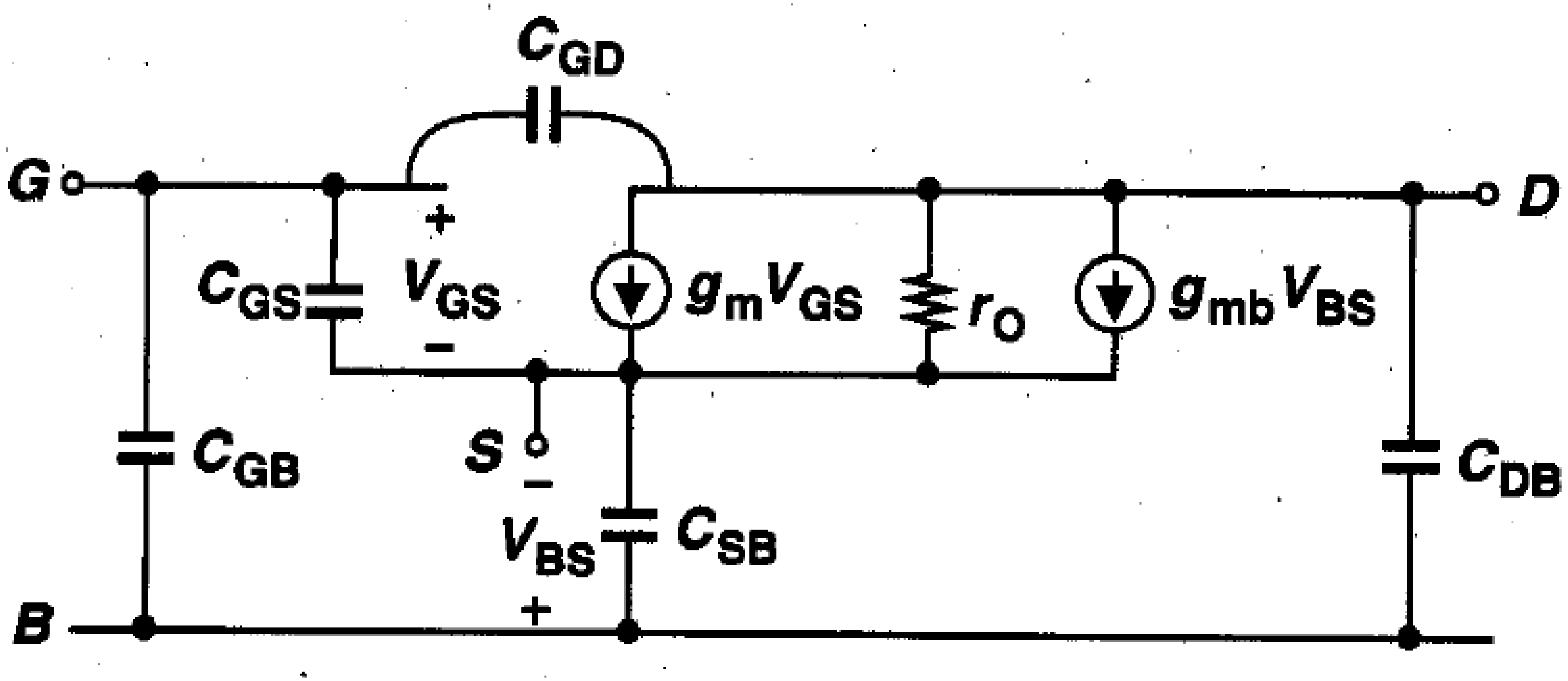


MOS Small signal model





$$
\begin{aligned}
r_O &= \frac{\partial V_{DS}}{\partial I_D} \\
&= \frac{1}{\partial I_D / \partial V_{DS}}. \\
&= \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \cdot \lambda} \\
&\approx \frac{1}{\lambda I_D}.
\end{aligned}
$$



NMOS Model

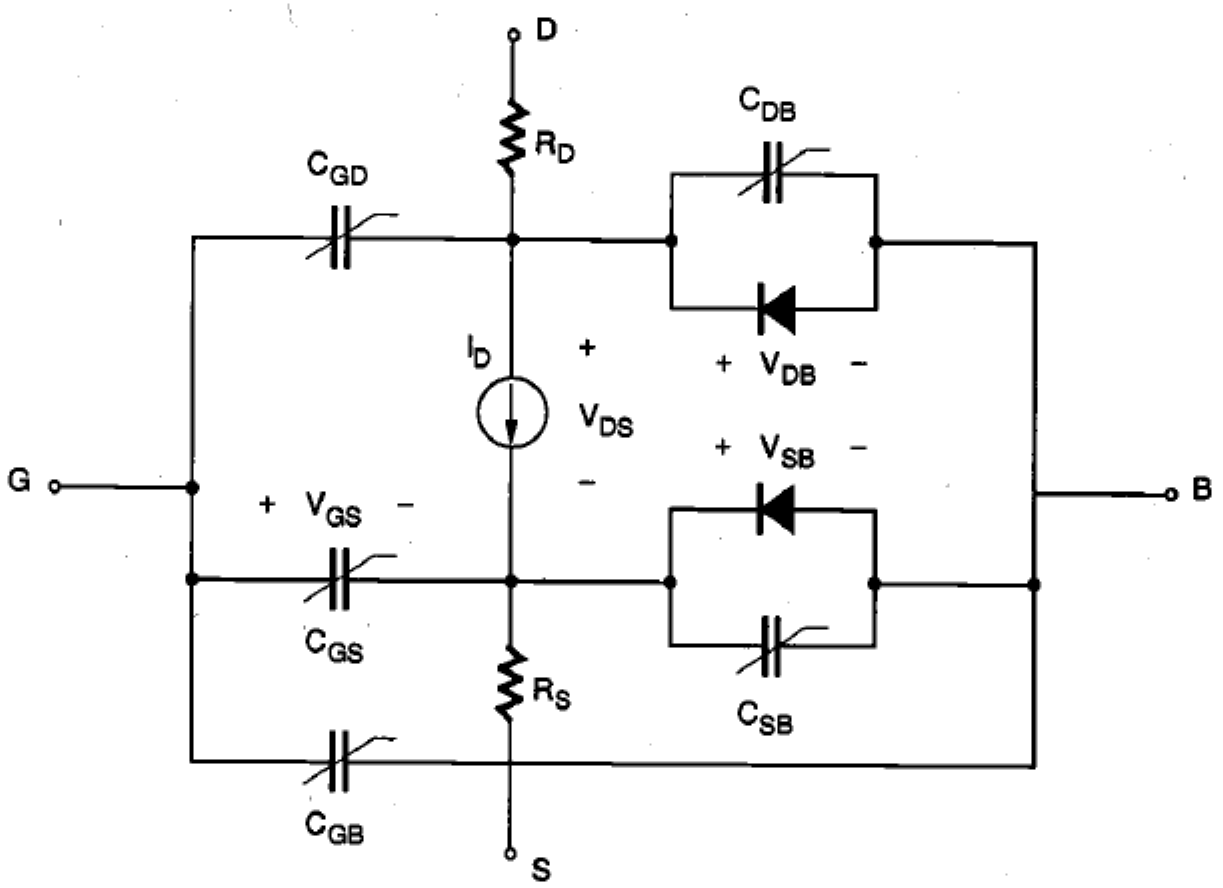
LEVEL = 1 VTO = 0.7 GAMMA = 0.45 PHI = 0.9
NSUB = 9e+14 LD = 0.08e−6 UO = 350 LAMBDA = 0.1
TOX = 9e−9 PB = 0.9 CJ = 0.56e−3 CJSW = 0.35e−11
MJ = 0.45 MJSW = 0.2 CGDO = 0.4e−9 JS = 1.0e−8

PMOS Model

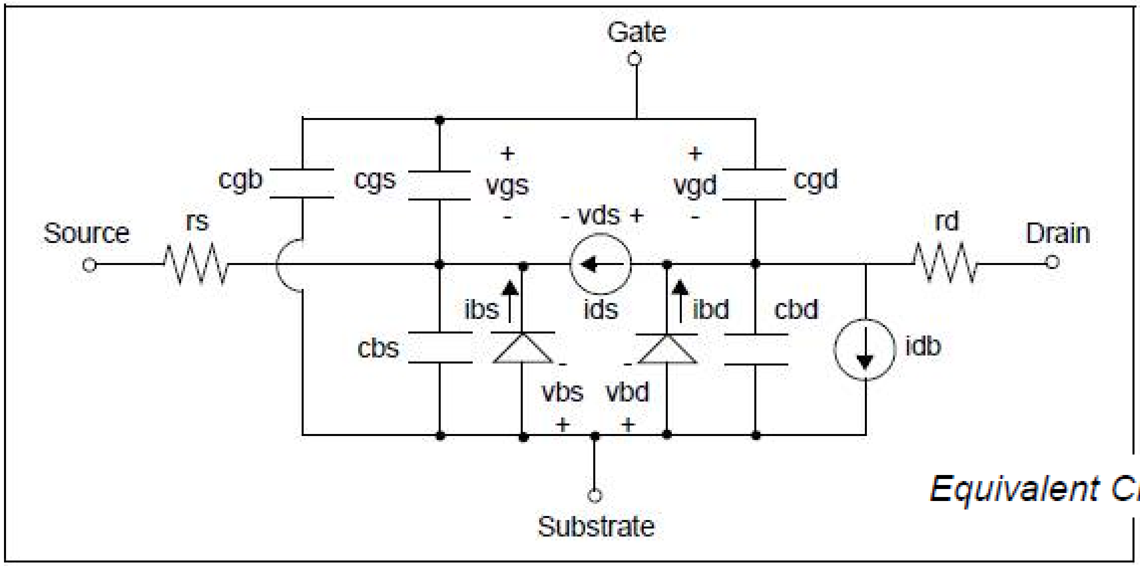
LEVEL = 1 VTO = −0.8 GAMMA = 0.4 PHI = 0.8
NSUB = 5e+14 LD = 0.09e−6 UO = 100 LAMBDA = 0.2
TOX = 9e−9 PB = 0.9 CJ = 0.94e−3 CJSW = 0.32e−11
MJ = 0.5 MJSW = 0.3 CGDO = 0.3e−9 JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

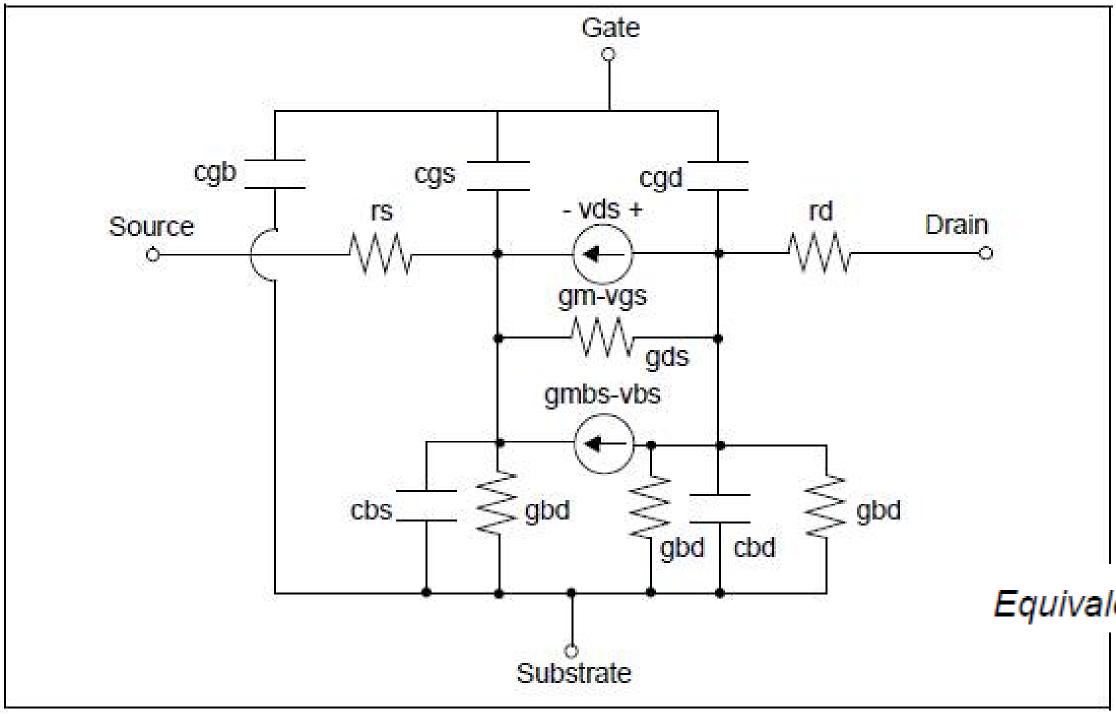
The equivalent circuit structure of the NMOS LEVEL 1 model



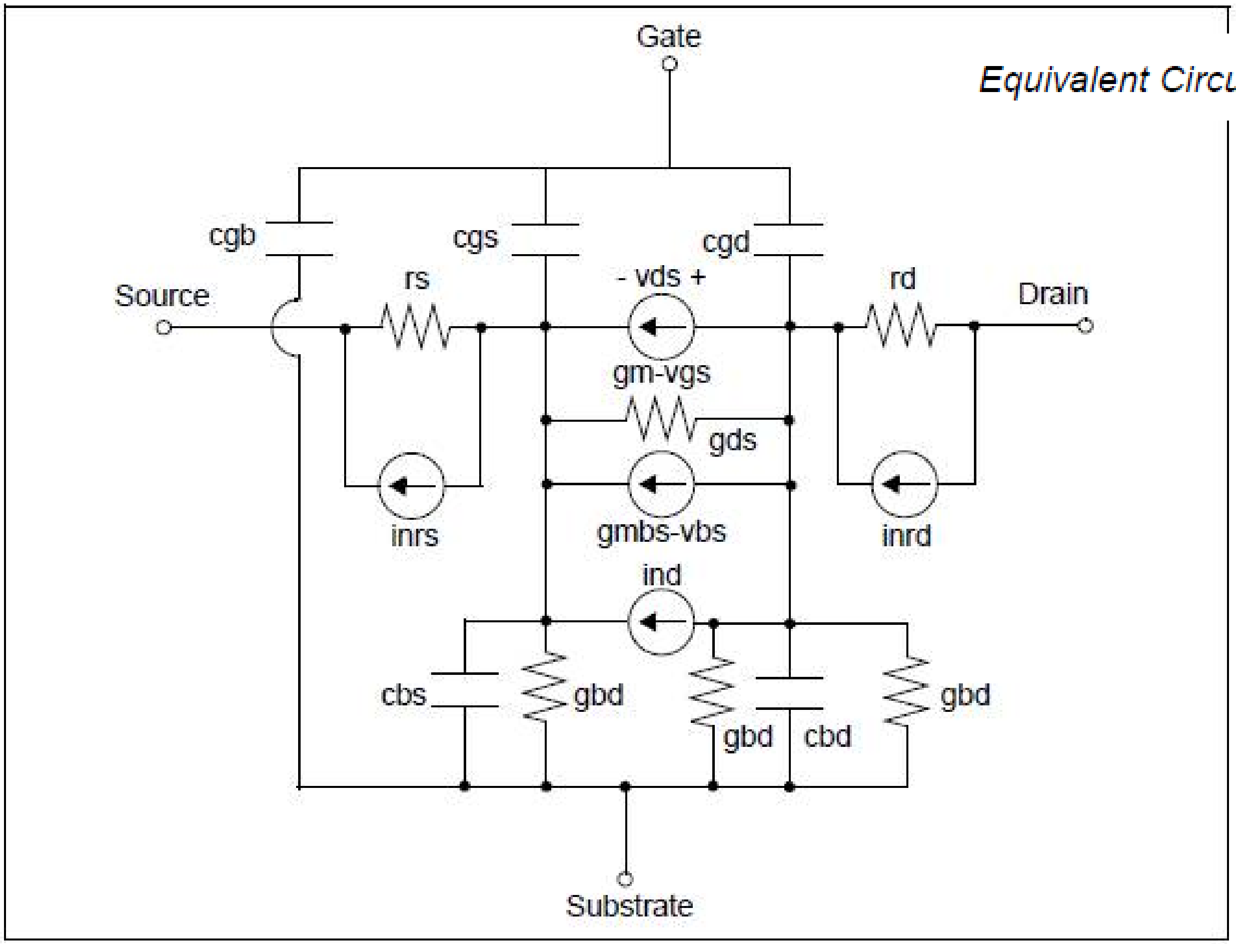
Why two different looks



Equivalent Circuit, MOSFET Transient Analysis



Equivalent Circuit, MOSFET AC Analysis



Equivalent Circuit, MOSFET AC Noise Analysis

idb	Drain-to-bulk impact ionization current
ind	Drain-to-source equivalent noise circuit
inrd	Drain resistor equivalent noise circuit
inrs	Source resistor equivalent noise circuit

Linear region

$$I_D = \frac{k'}{2} \cdot \frac{W}{L_{eff}} \cdot \left[2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \cdot (1 + \lambda \cdot V_{DS})\ for\ \ V_{GS} \geq V_T$$

$$and\ V_{DS} < V_{GS}\text{-}V_T$$

Saturation region

$$I_D = \frac{k'}{2} \cdot \frac{W}{L_{eff}} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})\ for\ \ V_{GS} \geq V_T$$

$$and\ V_{DS} \geq V_{GS}\text{-}V_T$$

The threshold voltage

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right)$$

$$L_{eff} = L - 2 \cdot L_D$$

$$k' = \mu \cdot C_{ox} \text{ where } C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\gamma = \frac{\sqrt{2 \cdot \varepsilon_{Si} \cdot q \cdot N_A}}{C_{ox}}$$

$$2\phi_F = 2\frac{kT}{q} \cdot \ln\left(\frac{n_i}{N_A}\right)$$

"Electrical Parameters"

- there are 5 parameters that fully characterize the base model

PARAMETER	DESCRIPTION
KP	k', transconductance
VTO	V_{TO}, zero substrate bias threshold
GAMMA	γ, substrate-bias coefficient
PHI	$\lvert 2\phi_F \rvert$, surface potential
LAMBDA	λ, channel length modulation coefficient

"Physical Parameters"

- there are parameters that describe the shape and material properties of the device

Parameter	Description
U0	u_n, electron mobility
TOX	t_{ox}, oxide thickness
NSUB	N_A, doping concentration
LD	L_D, lateral diffusion

$K'=27.6\mu A/V^2$	KP=27.6U
$V_{T0}=1.0V$	VTO=1
$\gamma=0.53V^{1/2}$	GAMMA=0.53
$2\phi F=-0.58$	PHI=0.58
$\lambda=0$	LAMBDA=0
$\mu_n=800cm^2/Vs$	UO=800
$t_{ox}=100nm$	TOX=100E-9
$N_A=10^{15}cm^{-3}$	NSUB=1E15
$L_D=0.8\mu m$	LD=0.8E-6

- The threshold voltage of a MOS transistor (Vth is V_{GS} required to strongly invert the surface of the substrate under the gate.) is calculated like that of a MOS structure with one slight modification in Q_B.

$$Q_B = \sqrt{2\mathrm{q}\ \ \mathrm{N}_{\mathrm{sub}}\ \ \varepsilon_{\mathrm{sub}} \,|\, 2\,\phi_F - V_{SB} \,|}$$

Where V_{SB} is the source to bulk voltage.

- For circuit analysis:

$$V_{th} = V_{T0} + \gamma(\sqrt{|\,2\phi_F - V_{SB}\,|} - \sqrt{|\,2\phi_F\,|})$$

Where γ is called body effect coefficient = $\dfrac{\sqrt{2q\ N_{sub}\varepsilon_{sub}}}{C_{ox}}$

V_{T0} = the threshold voltage with V_{SB} =0 i.e. with out the body effect.

For Detail calc. Pg 59 in book CMOS digital integrated circuit by Kang

- notice that these parameters are redundant with the Electrical parameters since these quantities are used to calculate k', V_{T0}, γ, $|2\phi_F|$, and λ these allow you to get further into the details of the fabrication to see its effect on performance
- However, the “Electrical Parameters” OVERRIDE the “Physical Parameters”
- this means you wouldn’t supply both if you really want to see the effect of a physical parameters on the performance of the device.
- You would need to remove the electrical parameter.

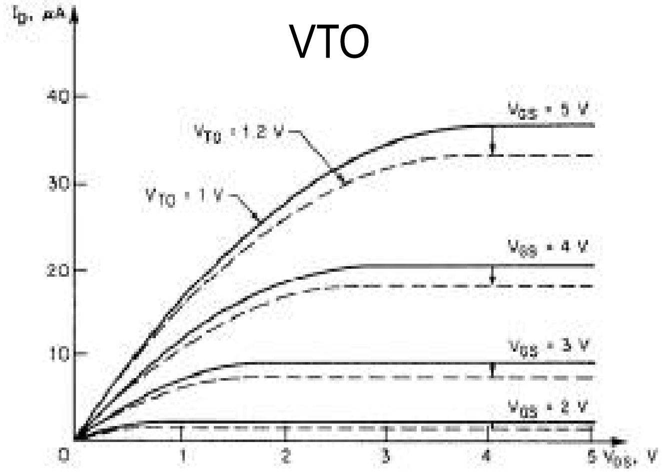
“Parasitic Parameters”

- these are the capacitances and resistances of the material

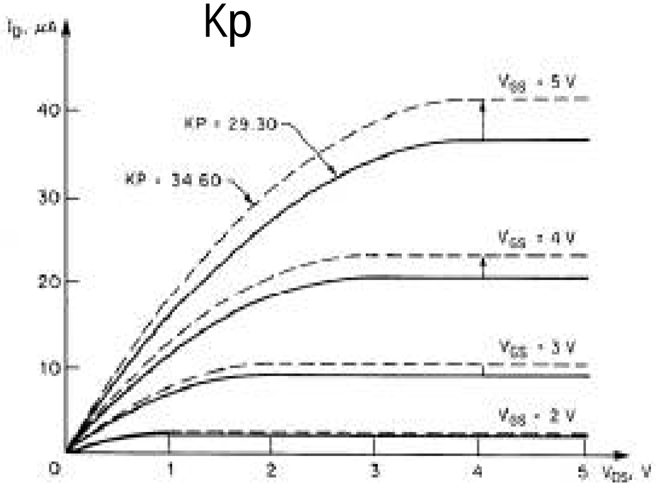
Parameter	Description
CJ	C_{J0}, zero-bias bulk capacitance per area
CJSW	C_{J0sw}, zero-bias sidewall capacitance per area

Variation of the drain current with model parameter

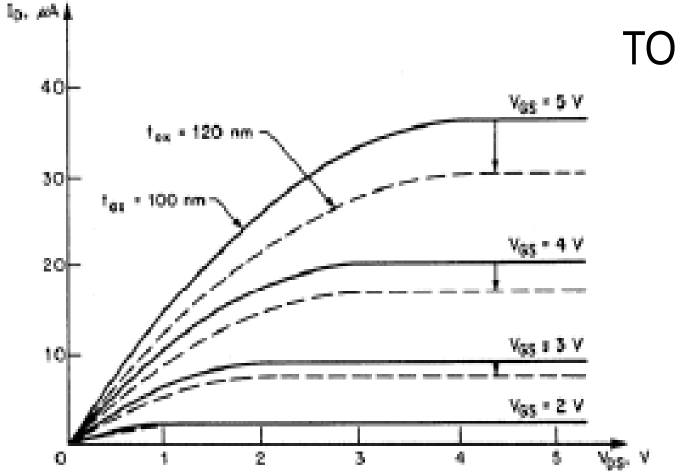
VTO



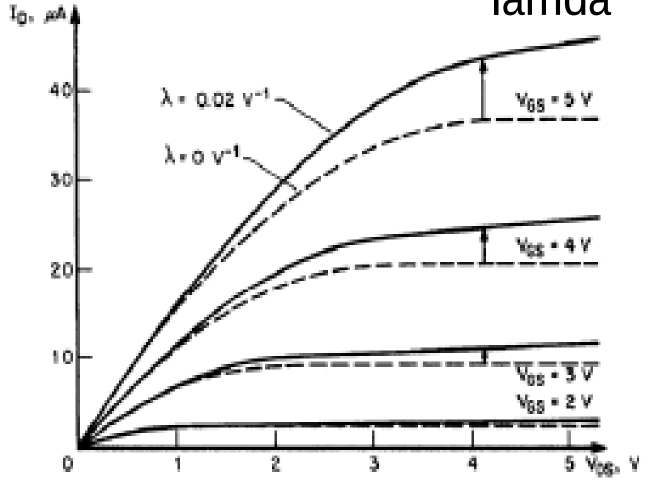
Kp



TOX



lamda



- Level 1 model is also known as **SHICHMAN and HODGES model**

Level 2 SPICE Modeling

Level 2 adds the following behavior to the Level 1 model

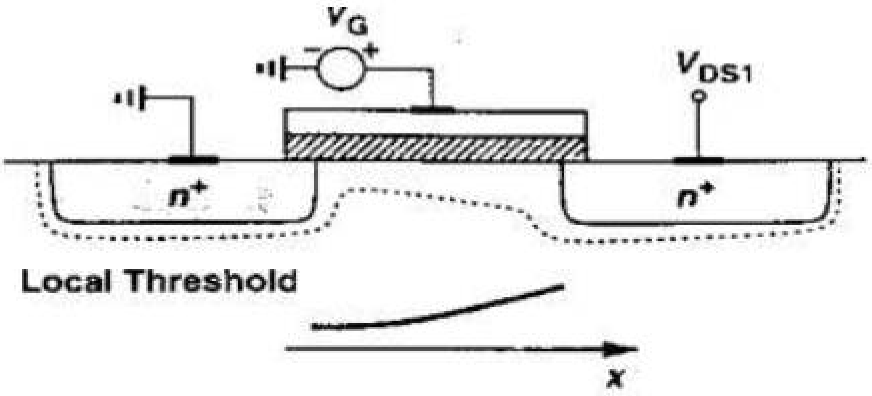
1) Variation of the bulk depletion charge dependence on the channel voltage (we assumed it was constant in Level 1
2) Variation of electron mobility (u_n) with the applied E-field
3) Variation of effective Channel Length in Saturation model
4) Carrier Velocity Saturation
5) Sub-threshold Conduction

- We also have the ability to indicate which level we want to use. For example, you can have a Level 2 model, but in the initalization you say:

```
M1   D   G   S   B    NMOD              (Level=1 L=1U  W=10U)
```

  This will tell the simulator to ignore all the parameters associated with Level 2 or higher accuracy.

- An assumption we made in square law characteristics is the constant threshold voltage along the channel . This assumption is not correct even for long channel devices because charge in depletion layer varies according to the local voltage



The LEVEL 2 model equation

$$I_D = \frac{k'}{(1-\lambda \cdot V_{DS})} \cdot \frac{W}{L_{eff}} \cdot \left\{ \left(V_{GS} - V_{FB} - |2\phi_F| - \frac{V_{DS}}{2} \right) \cdot V_{DS} - \frac{2}{3} \cdot \gamma \cdot \left[\left(V_{DS} - V_{BS} + |2\phi_F| \right)^{3/2} - \left(-V_{BS} + |2\phi_F| \right)^{3/2} \right] \right\}$$

The saturation voltage

$$V_{DSAT} = V_{GS} - V_{FB} - |2\phi_F| + \gamma^2 \cdot \left(1 - \sqrt{1 + \frac{2}{\gamma^2} \cdot (V_{GS} - V_{FB})} \right)$$

The saturation mode current

$$I_D = I_{Dsat} \cdot \frac{1}{(1\text{-}\lambda \cdot V_{DS})}$$

The zero bias threshold voltage

$$V_{T0} = \Phi_{GC} - \frac{q \cdot N_{ss}}{C_{ox}} + |2\phi_F| + \gamma \sqrt{|2\phi_F|}$$

variation of channel length in saturation mode

$$L'_{eff} = L_{eff} - \Delta L$$

$$\Delta L = \sqrt{\frac{2 \cdot \varepsilon_{Si}}{q \cdot N_A}} \cdot \left[\frac{V_{DS} - V_{DSAT}}{4} + \sqrt{1 + \left(\frac{V_{DS} - V_{DSAT}}{4} \right)^2} \right]$$

The empirical channel length shortening coefficient

$$\lambda = \frac{\Delta L}{L_{eff} \cdot V_{DS}}$$

Subthreshold conduction

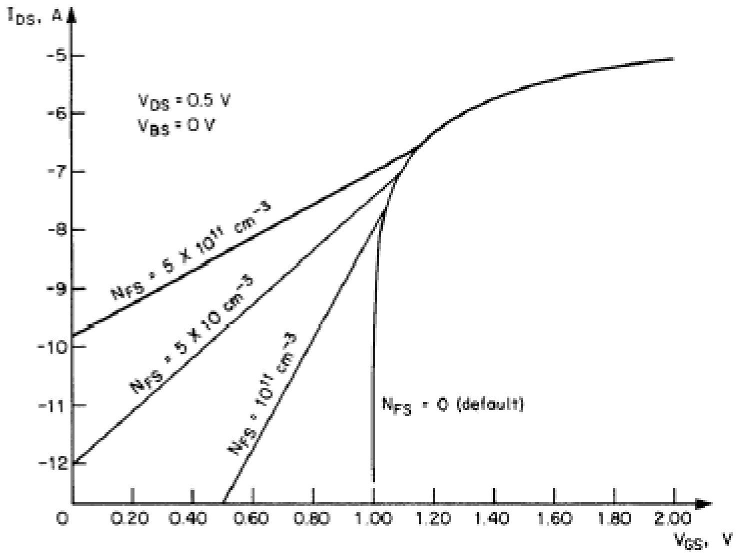
- For $V_{GS}<V_T$, there is a channel current even when the surface is not in strong inversion
- This subthreshold current
  - Due mainly to diffusion between and the channel
  - Becoming an increasing concern for deep-sub-micron designs
- The model implemented in SPICE introduces an exponential, semi-empirical dependence of the drain current on V_{GS} in the *weak inversion region*

$$I_D(\text{weak inversion}) = I_{on} \cdot e^{(V_{GS}-V_{on})\cdot\left(\frac{q}{nkT}\right)}$$

I_{on} is the current in strong inversion for $V_{GS} = V_{on}$

the voltage V_{on} is found as

$$V_{on} = V_T + \frac{nkT}{q} \quad where\ n = 1 + \frac{q \cdot N_{FS}}{C_{ox}} + \frac{C_d}{C_{ox}}$$



The LEVEL 3 model equations

- The LEVEL 3 model has been developed for simulation of short channel MOS transistor
  - Quite precisely for channel lengths down to 2μm
  - The current-voltage equation in the linear region has been simplified with a Taylor series expansion
  - The majority of the LEVEL 3 model equations are empirical
    - To improve the accuracy of the model
    - To limit the complexity of the calculation

$$I_D = \mu_s \cdot C_{ox} \cdot \frac{W}{L_{eff}} \cdot \left(V_{GS} - V_T - \frac{1+F_B}{2} \cdot V_{DS} \right) \cdot V_{DS}$$

$$where\ F_B = \frac{\gamma \cdot F_s}{4 \cdot \sqrt{|2\phi_F| + V_{SB}}} + F_n$$

The empirical parameter F_B express the dependence of the bulk depletion charge

The V_T. F_s, and μ_s are influenced by the short - channel effects

The F_n is influenced by the narrow - channel effects

$$\mu_s = \frac{\mu}{1+\theta \cdot (V_{GS}\text{-}V_T)}$$

The decrease in the effective mobility with the average lateral electrical field

$$\mu_{eff} = \frac{\mu_s}{1+\mu_s \cdot \frac{V_{DS}}{v_{\max} \cdot L_{eff}}}$$

Comparison of the SPICE MOSFET models

- The LEVEL 1 model
  - Not very precise
  - Quick and rough estimate of the circuit performance without much accuracy
- THE LEVEL 2 model
  - Require a larger time
  - May occasionally cause convergence problems in the Newton-Raphson algorithm used in SPICE
- THE LEVEL 3 model
  - The CPU time needed for model evaluation is less and the number of iterations are significantly fewer for the LEVEL three model
  - Disadvantage
    - The complexity of calculating some of its parameters

DC model selector:

- LEVEL=1 (default) is the Schichman-Hodges model.
- LEVEL=2 is the Grove-Frohman model.
- LEVEL=3 is an empirical model.
- LEVEL=4 is a modified version of Level 2.
- LEVEL=5 is the IDS model with enhancement and depletion modes.
- LEVEL=6 is the Lattin-Jenkins-Grove model us using ASPEC-style parasitics.
- LEVEL=7 is the Lattin-Jenkins-Grove model us using SPICE-style parasitics.
- LEVEL=8 is an advanced model using finite differences.
- LEVEL=13 is the University of California (UC) Berkeley BSIM1 model.
- LEVEL=27 is the SOSFET model.
- LEVEL=28 is a Synopsys proprietary model, based on the UC Berkeley BSIM1 model, Level 13.
- LEVEL=38 is the Cypress Depletion model.
- LEVEL=39 is the UC Berkeley BSIM2 model.
- LEVEL=40 is the Hewlett-Packard amorphous-silicon Then-Film Transistor (a-Si TFT) model.
- LEVEL=47 is the UC Berkeley BSIM3 version 2 model.
- LEVEL=49 is a Synopsys proprietary model, based on the UC Berkeley BSIM3 version 3 model, Level 53.
- LEVEL=50 is the Philips MOS9 model.
- LEVEL=53 is the original UC Berkeley BSIM3 version 3 model, not modified as Level 49 is.
- LEVEL=54 is the UC Berkeley BSIM4 model.
- LEVEL=55 is the EPFL-EKV model.
- LEVEL=57 is the UC Berkeley BSIM3-SOI Partially-Depleted (PD) model.
- LEVEL=58 is the University of Florida SOI model.
- LEVEL=59 is the UC Berkeley BSIM3-SOI Fully-Depleted (FD) model.
- LEVEL=60 is the UC Berkeley BSIM3-SOI Dynamically-Depleted (DD) model.
- LEVEL=61 is the Rensselaer Polytechnic Institute (RPI) a-Si TFT model.
- LEVEL=62 is the Rensselaer Polytechnic Institute (RPI) poly-silicon Thin-Film Transistor (Poli-Si TFT) model.
- LEVEL=63 is the Philips MOS11 model.
- LEVEL=64 is the Hiroshima STARC IGFET (HiSIM) model.

SPICE Modeling in BSIM

- Berkeley Short-Channel IGFET Model
- This is the most commonly used model for accurate simulations.
- This is a totally empirical model which reduces the curve fitting parameters
- This actually reduces simulation time over the Level 3 models.

BSIM-CMG (Common Multi-Gate)
BSIM-IMG (Independent Multi-Gate) the only model published without source-code (whose publication is foreseen for July 13, 2021)
BSIM-SOI (Silicon-on-Insulator)
BSIM-BULK, formerly BSIM6,
BSIM4,used for 0.13 μm to 20 nm nodes,
BSIM3, a predecessor of BSIM4.

BSIM series

- In the previous models (level 1-3)the device behaviour is expressed by means of equation that originated from physical operation.
- But nowadays the transistors are scaled to submicron levels, so became difficult to introduce physical equations that is both accurate and computationally efficient.
- It uses numerical empirical parameters so as to simplify the equations by compromising with actual device operations

Gate oxide capacitance

- SPICE uses a simple gate oxide capacitance model that represents the charge storage effect by three nonlinear two-terminal capacitor: C_{GB}, C_{GS} and C_{GD}
- The geometry information required for the calculation of gate oxide capacitance are:
  - Gate oxide thickness TOX
  - Channel width W
  - Channel length L
  - Lateral diffusion LD
- The capacitances CGBO, CGSO, and CGDO, which are specified in the .MODEL statement, are the overlap capacitances between the gate and the other terminals outside the channel region

Junction capacitance

$$C_{SB} = \frac{C_j \cdot AS}{\left(1 - \frac{V_{BS}}{\phi_0}\right)^{M_j}} + \frac{C_{jsw} \cdot PS}{\left(1 - \frac{V_{BS}}{\phi_0}\right)^{M_{jsw}}}$$

$$C_{DB} = \frac{C_j \cdot AD}{\left(1 - \frac{V_{BD}}{\phi_0}\right)^{M_j}} + \frac{C_{jsw} \cdot PD}{\left(1 - \frac{V_{BD}}{\phi_0}\right)^{M_{jsw}}}$$

C_j : the zero - bias depletion capacitance per unit area at the bottom of the junction

C_{jsw} : the zero - bias depletion capzcitance per unit length at the sidewall junctions

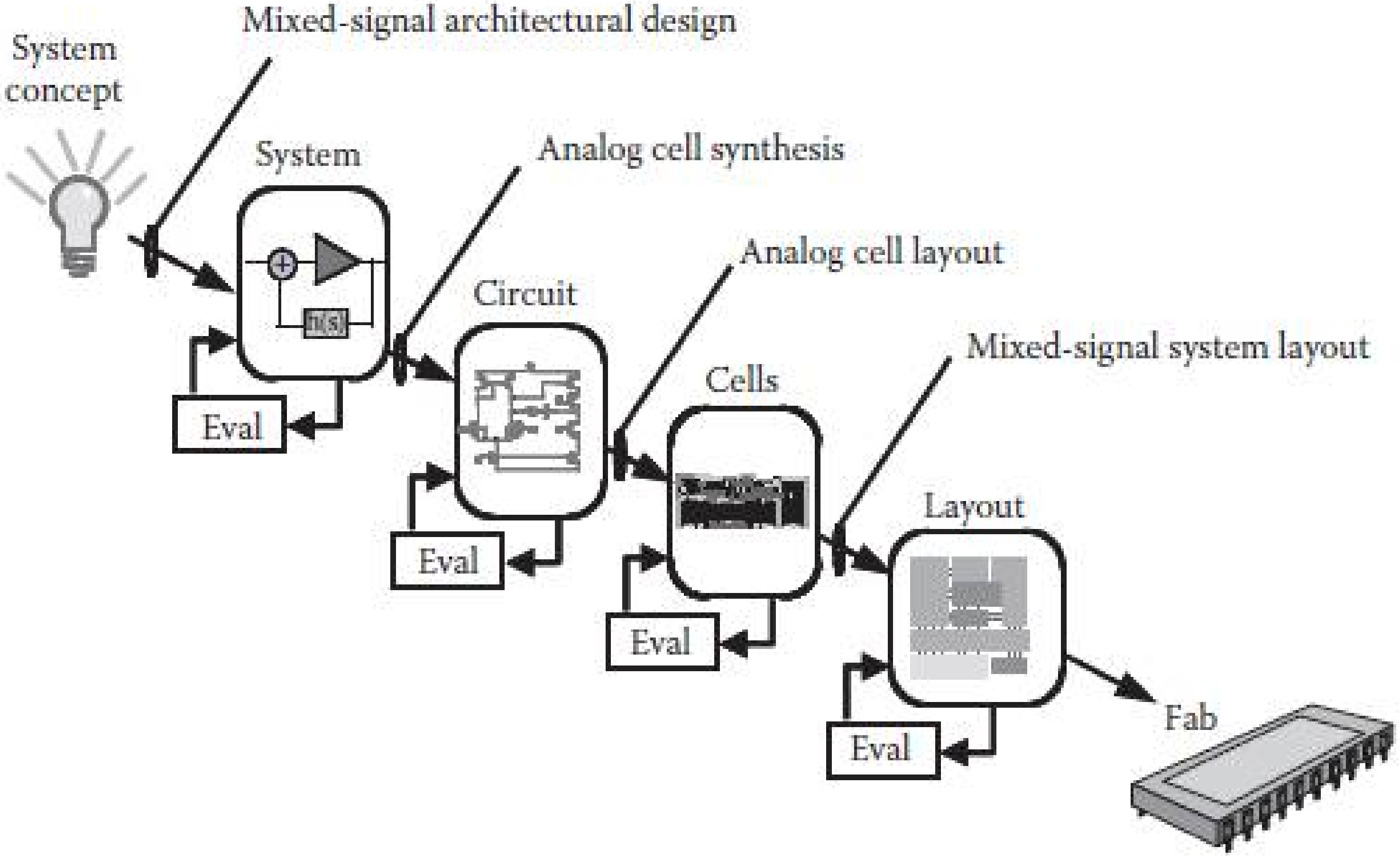
Modeling

Types of Modeling

During the verification of a large integrated circuit, it is common to use a variety of modeling formats in the verification process. Common formats can include:

- **Device based design (Spectre, SPICE)** – schematics built using process-specific devices is the standard transistor-level design technique. A macromodeling approach can also be used that uses generic elements and dependent sources to define simple block operations.
- **Analog modeling (Verilog-A)** – defines an analog description of relationships as current/ voltage equations to be solved by the analog solver.
- **Mixed-signal modeling (Verilog-AMS [7], VHDL-AMS [8])** – allows linked descriptions of analog operation of electrical portions and digital operation of logical portions of the block's operation.
- **Discrete real number modeling (Verilog-AMS, VHDL [6], SystemVerilog [11])** – uses a discrete solver for the model definition. This replaces electrical operations with the computation of real output values in terms of real input values to define primary input-to-output functionality. It typically ignores impedance effects.
- **Logic modeling (Verilog [5], VHDL, SystemVerilog)** – model defines discrete logic data flow, ignores analog operations.

Top-down view of the mixed-signal IC design process



Models for circuit design

- Transistor models are used for almost all modern electronic design work.
- Analog circuit simulators such as SPICE use models to predict the behavior of a design.
- LT SPICE is getting popularity too.
- Most design work is related to IC designs which have a very large tool cost, primarily for the photo masks used to create the devices, and there is a large economic incentive to get the design working without any iterations.
- Device models must include effect of various parameters on design like:
  - Width & length
  - Inter-digitation
  - Proximity to other devices
  - Transient and DC current-voltage characteristics
  - Parasitic device capacitance
  - Resistance and inductance
  - Time delays
  - Temperature effects

Device Modeling

- It is extremely important to have a valid device modeling & simulation design prior to the device fabrication technology & design iteration are expensive and post fabrication tuning is not a fun.

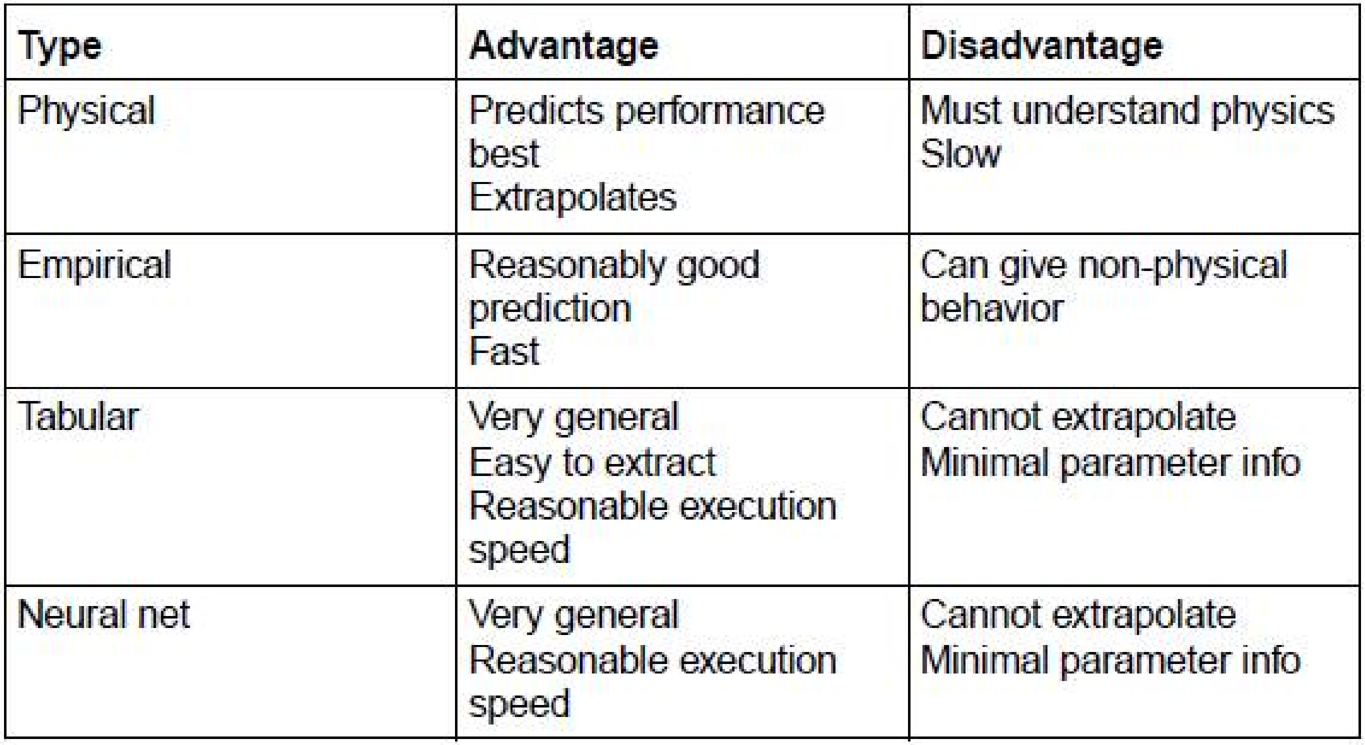
- Modern device designing is very complex, so it is difficult to predict performance characteristics of device without accurate computer models.

- Device modeling actually describes the principal methods of representing and analyzing devices.

- Device modeling is useful in device design, production control and performance analysis.

Transistor – Large signal nonlinear models

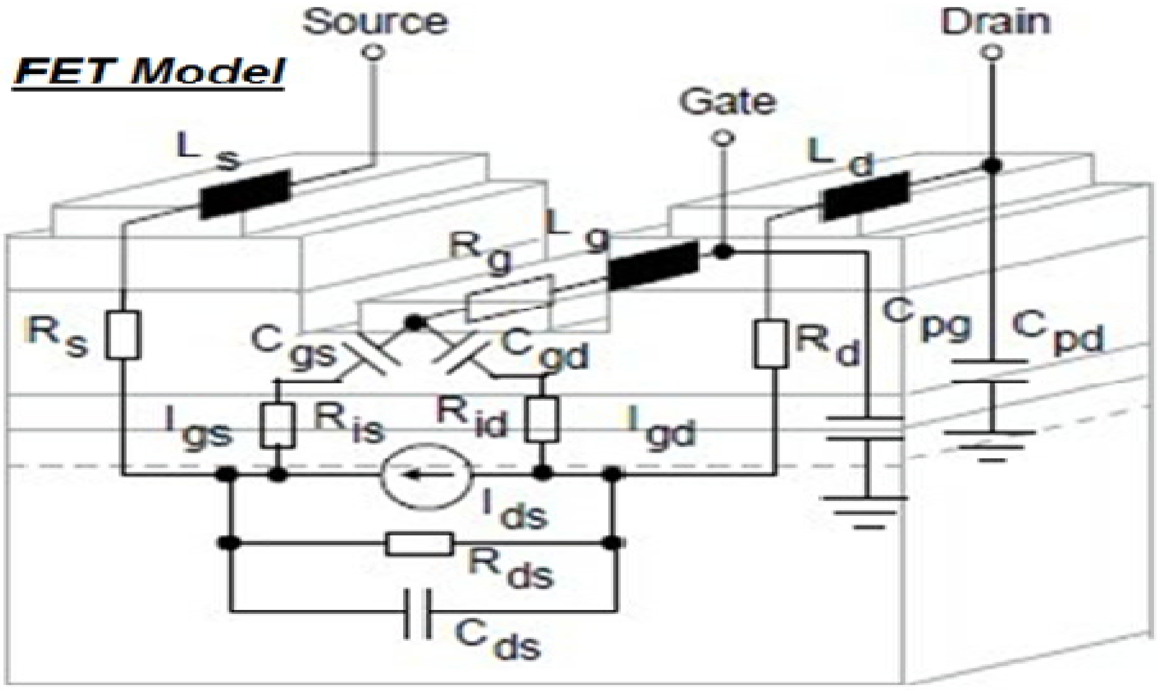
- Large signal transistor models (non-linear models) fall into three main types.
  - Physical models
  - Empirical models
  - Tabular models



Type	Advantage	Disadvantage
Physical	Predicts performance best Extrapolates	Must understand physics Slow
Empirical	Reasonably good prediction Fast	Can give non-physical behavior
Tabular	Very general Easy to extract Reasonable execution speed	Cannot extrapolate Minimal parameter info
Neural net	Very general Reasonable execution speed	Cannot extrapolate Minimal parameter info

Physical models

- These are models based upon device physics, which relies on the approximate modeling of physical phenomena within a transistor.
- Parameters within these models are based upon physical properties such as
  - Oxide thicknesses, Substrate doping concentrations, Carrier mobility, etc.

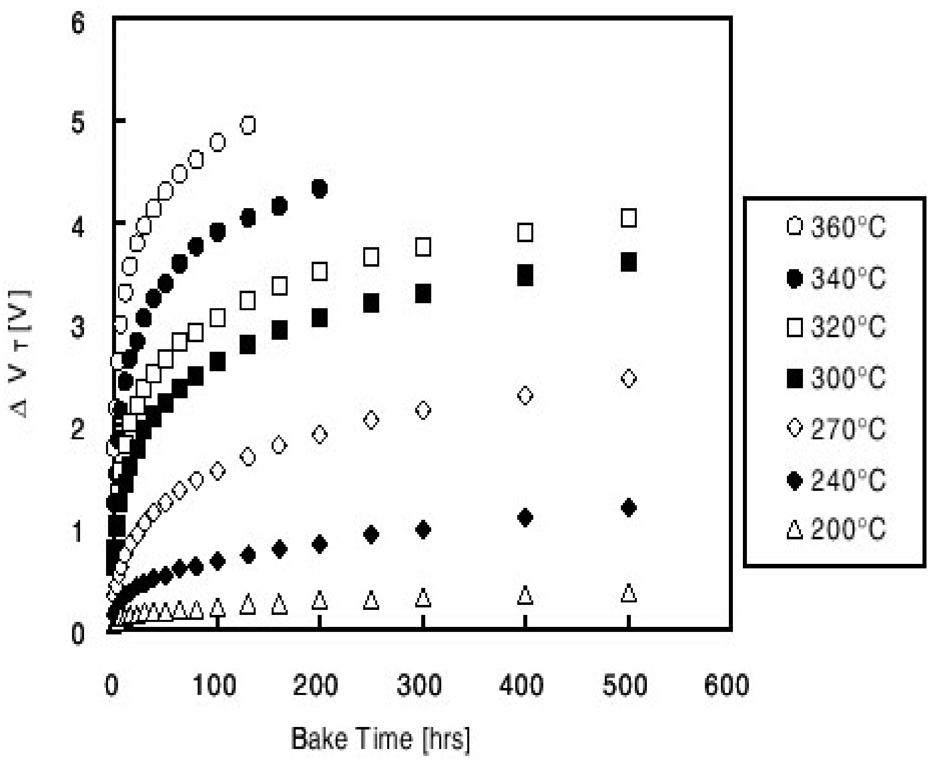


Cont..

- Physical device models are solved using either bulk carrier transport equations (the semiconductor equations), solutions to the Boltzmann transport equation or quantum transport concepts.
  - Bulk transport solutions have satisfied most device models
  - Boltzmann and quantum transport solutions have provided a strong insight into the detailed device physics.
- The understanding of material properties, physical boundary conditions (such as surface physics, contact properties and device geometry) and device-circuit interaction are steadily improving, allowing more intricate models to be developed.

Empirical models

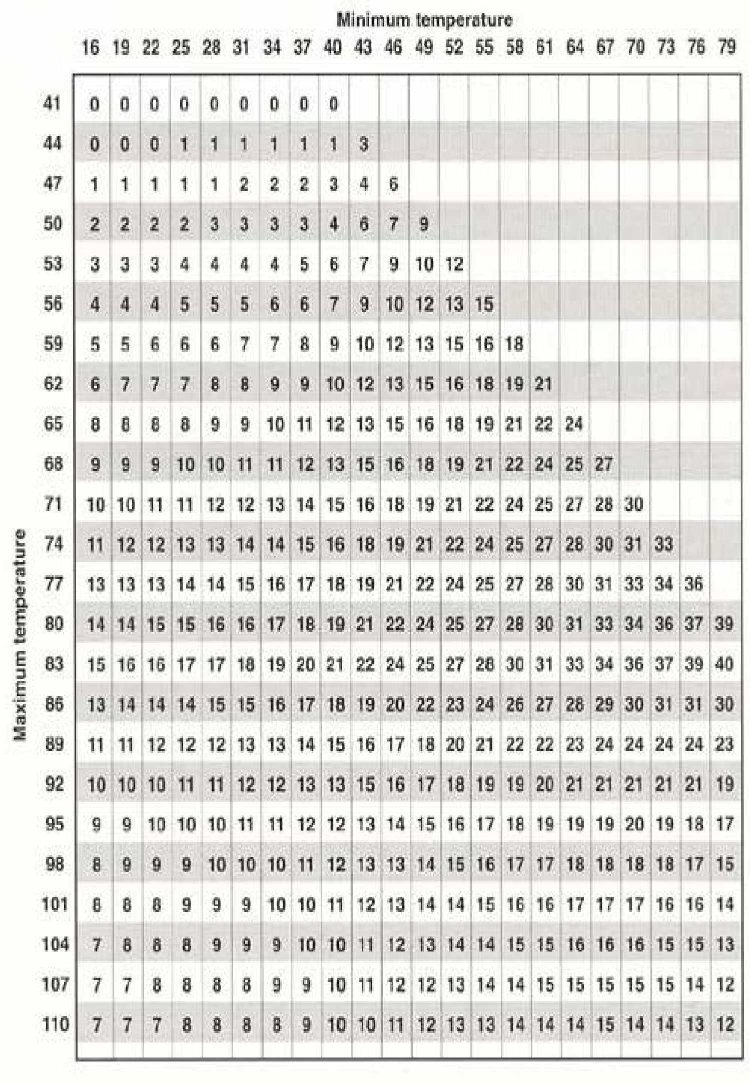
- Empirical models are based upon curve fitting, subjected to the parameter and values which can fit describe the operation of the device (transistor).
- Unlike a physical model, empirical model parameters are not based fundamentals, they mostly depends on the fitting procedure used to find them.
- Fitting procedure is key to success of these models if they are to be used to extrapolate to designs lying outside the range of data to which the models were originally fitted.



Empirical model of carrier scattering on ionized impurity

Tabular models

- Tabular models are based on look-up table (LUT) form, by considering effect of one parameter to the other.
  - – Effect of parasitic components on drain current
- These values are indexed in reference to their corresponding bias voltage combinations.
- Thus, model accuracy is increased by inclusion of additional data points within the table.
- Limitation of these models is that they work best for designs that use devices within the table (interpolation) and are unreliable for devices outside the table (extrapolation).



	Minimum temperature																					
Maximum temperature	16	19	22	25	28	31	34	37	40	43	46	49	52	55	58	61	64	67	70	73	76	79
41	0	0	0	0	0	0	0	0	0													
44	0	0	0	1	1	1	1	1	1	3												
47	1	1	1	1	1	2	2	2	3	4	6											
50	2	2	2	2	3	3	3	3	4	6	7	9										
53	3	3	3	4	4	4	4	5	6	7	9	10	12									
56	4	4	4	5	5	5	6	6	7	9	10	12	13	15								
59	5	5	6	6	6	7	7	8	9	10	12	13	15	16	18							
62	6	7	7	7	8	8	9	9	10	12	13	15	16	18	19	21						
65	8	8	8	8	9	9	10	11	12	13	15	16	18	19	21	22	24					
68	9	9	9	10	10	11	11	12	13	15	16	18	19	21	22	24	25	27				
71	10	10	11	11	12	12	13	14	15	16	18	19	21	22	24	25	27	28	30			
74	11	12	12	13	13	14	14	15	16	18	19	21	22	24	25	27	28	30	31	33		
77	13	13	13	14	14	15	16	17	18	19	21	22	24	25	27	28	30	31	33	34	36	
80	14	14	15	15	16	16	17	18	19	21	22	24	25	27	28	30	31	33	34	36	37	39
83	15	16	16	17	17	18	19	20	21	22	24	25	27	28	30	31	33	34	36	37	39	40
86	13	14	14	14	15	15	16	17	18	19	20	22	23	24	26	27	28	29	30	31	31	30
89	11	11	12	12	12	13	13	14	15	16	17	18	20	21	22	22	23	24	24	24	24	23
92	10	10	10	11	11	12	12	13	13	15	16	17	18	19	19	20	21	21	21	21	21	19
95	9	9	10	10	10	11	11	12	12	13	14	15	16	17	18	19	19	19	20	19	18	17
98	8	9	9	9	10	10	10	11	12	13	13	14	15	16	17	17	18	18	18	18	17	15
101	8	8	8	9	9	9	10	10	11	12	13	14	14	15	16	16	17	17	17	16	16	14
104	7	8	8	8	9	9	9	10	10	11	12	13	14	14	15	15	16	16	16	15	15	13
107	7	7	8	8	8	8	9	9	10	11	12	12	13	14	14	15	15	15	15	15	14	12
110	7	7	7	8	8	8	8	9	10	10	11	12	13	13	14	14	14	15	14	14	13	12

Small-signal parameters

- A transistor's parameters represent its electrical properties.
- Engineers employ transistor parameters in production-line testing and in circuit design.
- A group of a transistor's parameters sufficient to predict circuit gain, input impedance, and output impedance are components in its small-signal model.
- Parameters used in small-signal circuits (two ports) adopt names related to the names of these circuits such as
  - Transmission parameters (T-parameters),
  - Hybrid-parameters (h-parameters),
  - Impedance parameters (z-parameters),
  - Admittance parameters (y-parameters), and
  - Scattering parameters (S-parameters).
- These parameters all can be evaluated using measured scattering parameter data.
- Scattering parameters (S parameters) can be measured for a transistor at a given bias point with a vector network analyzer.

Numerical Based

- Equivalent circuit models approach is generally limited in its applicability because of the DC bias, frequency dependence and the non-linear behavior of most devices with respect to signal level.
- The principal advantage of this technique is that it is easy to implement and analyze.

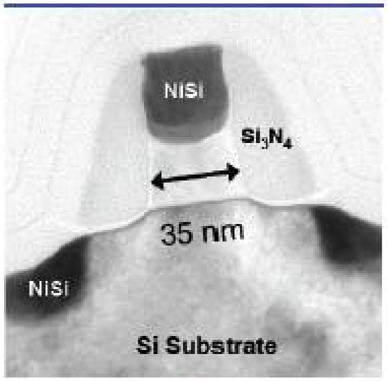
What is a compact model

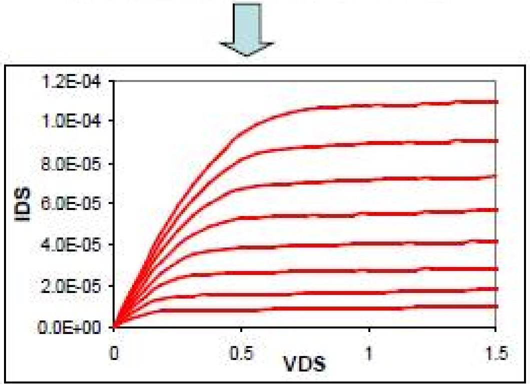
- Computationally efficient description of the terminal properties of a device as a function of terminal voltages.

$$[\{I\}, \{Q\}] = f(Vg, Vd, Vs, Vb)$$

- The compact model is implemented inside a circuit simulation engine.

Connecting the two worlds

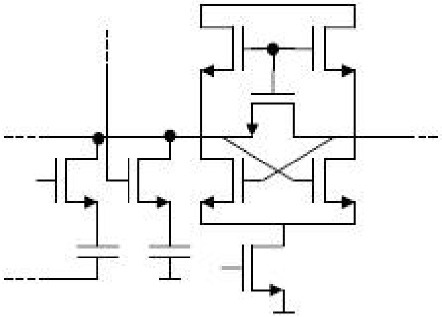




Technology / process development

- The process of making transistors, resistors, capacitors…etc, through a series of complex lithographical and chemical processes.

Bridge= Compact Model

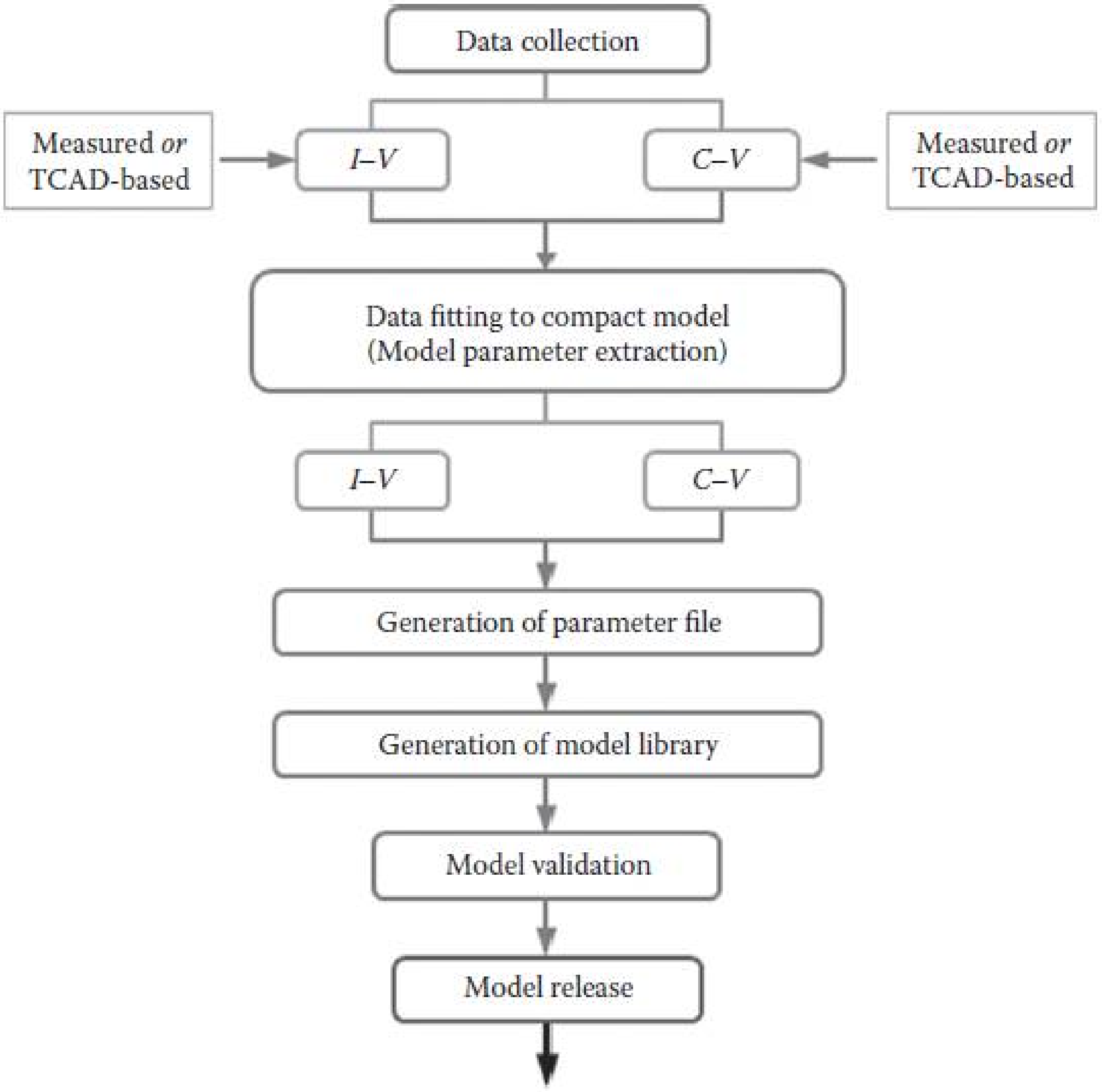


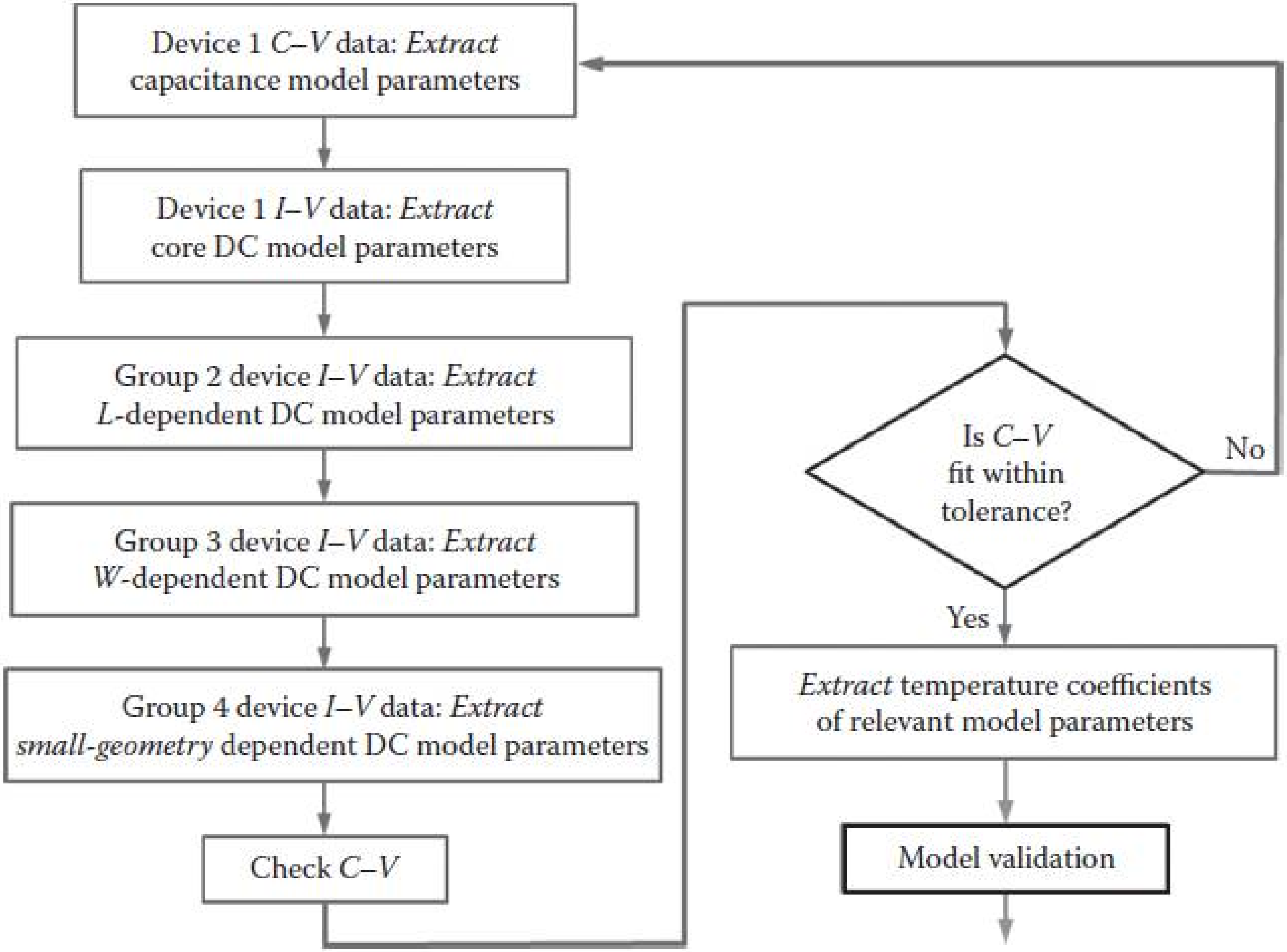
Design engineers use those transistors build logic circuits that perform specific functions.

IC design

- Design of an electrical network consisting of transistors, resistances, capacitances… etc, to perform a specified task.

With the objective of compact model standardization, an independent Compact Model Council, CMC was founded in 1996, consisting of many leading companies in the semiconductor industry. The charter of CMC is to promote the international, nonexclusive standardization of compact model formulations and the model interfaces. The CMC standardizes compact models for all major technologies to enhance the design efficiency, performs extensive model testing for model validation, and ensures robustness and accuracy of compact models for the latest technologies to shorten leading-edge design development cycle time. In 2013, CMC has become a part of an EDA standardization forum, Si2, to continue offering compact model standardization.

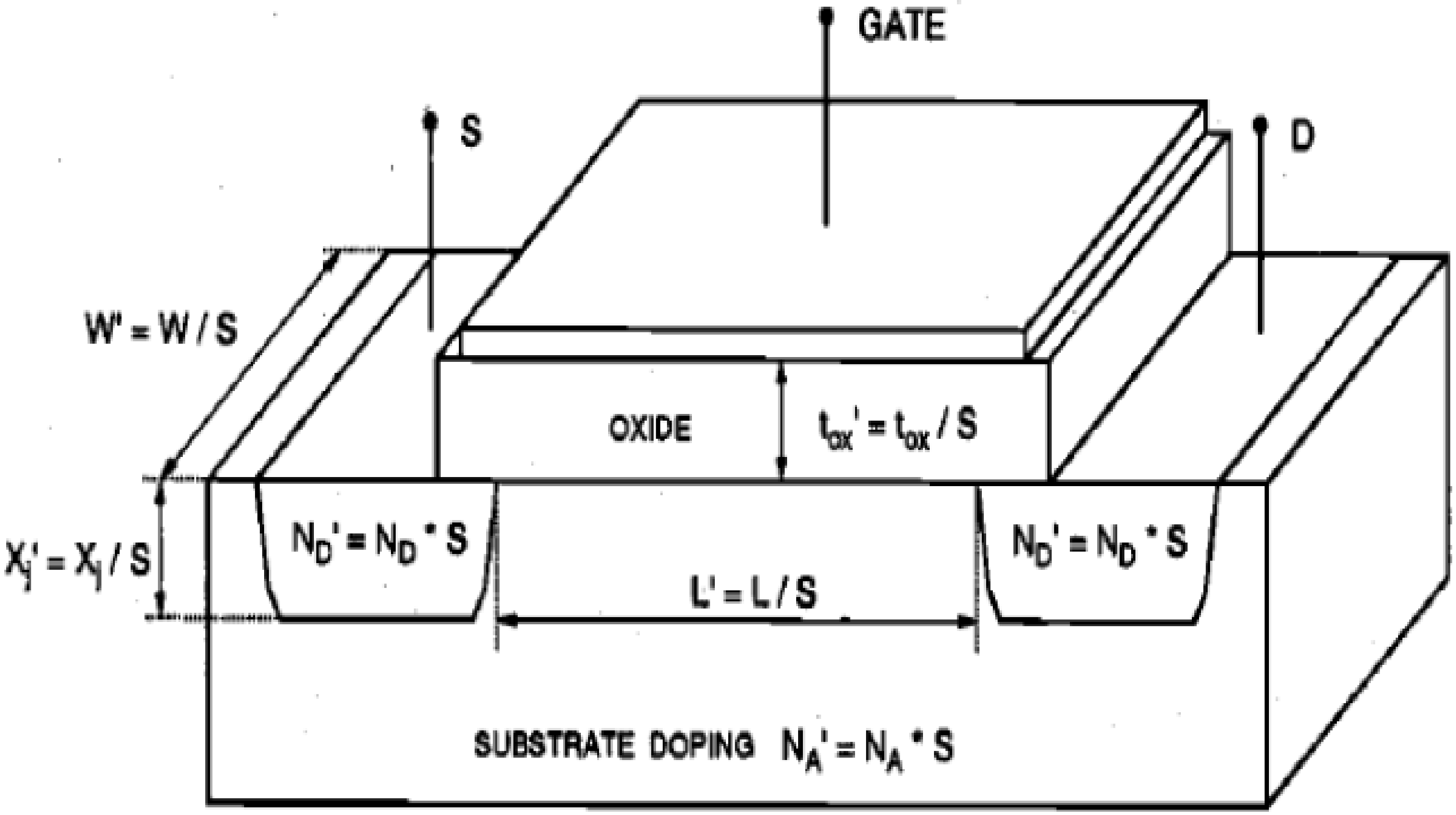

Data collection
Measured *or* TCAD-based
I–*V*
C–*V*
Measured *or* TCAD-based
Data fitting to compact model (Model parameter extraction)
I–*V*
C–*V*
Generation of parameter file
Generation of model library
Model validation
Model release


Device 1 C–V data: Extract capacitance model parameters
Device 1 I–V data: Extract core DC model parameters
Group 2 device I–V data: Extract L-dependent DC model parameters
Group 3 device I–V data: Extract W-dependent DC model parameters
Group 4 device I–V data: Extract small-geometry dependent DC model parameters
Check C–V
Is C–V fit within tolerance?
No
Yes
Extract temperature coefficients of relevant model parameters
Model validation

Scaling of MOS

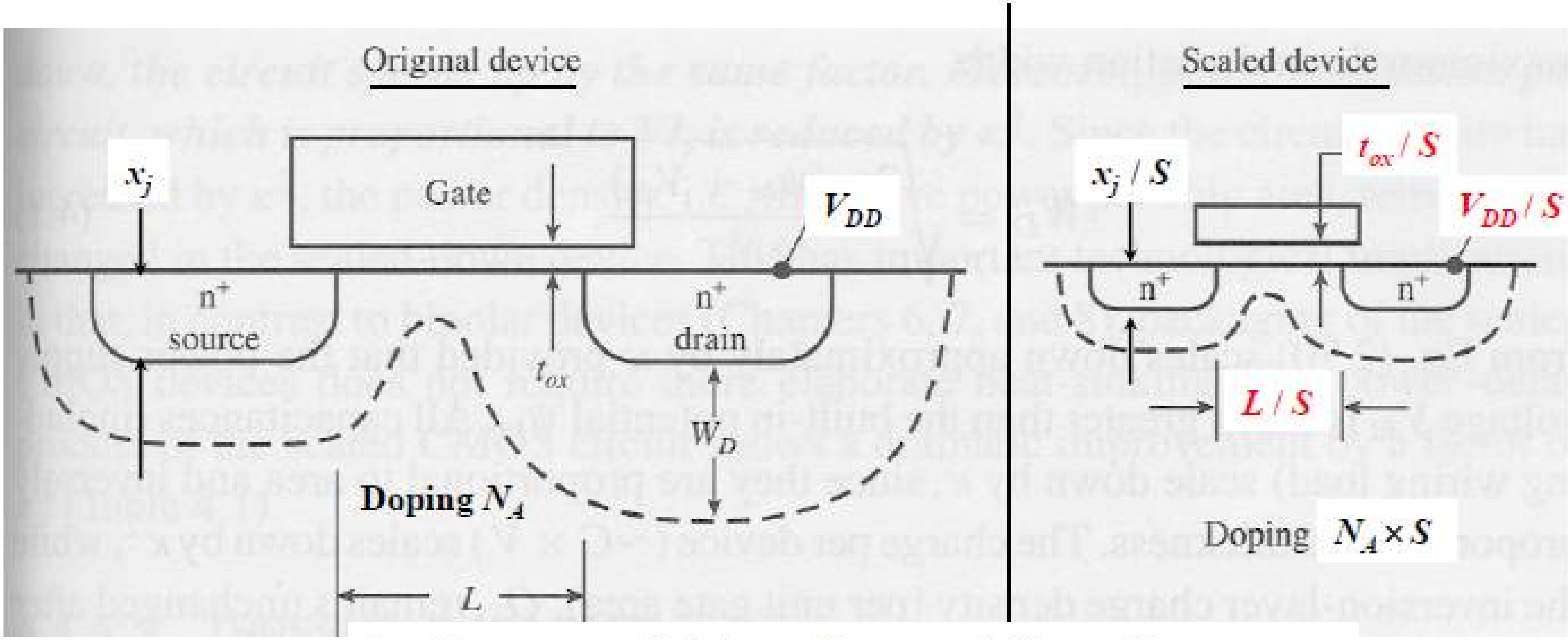
The design of high-density chips in MOS VLSI (Very Large Scale Integration) technology requires that the packing density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible. The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as *scaling*.

Scaling of MOS transistors is concerned with systematic reduction of overall dimensions of the devices as allowed by the available technology, while preserving the geometric ratios found in the larger devices. The proportional scaling of all devices in a circuit would certainly result in a reduction of the total silicon area occupied by the circuit, thereby increasing the overall functional density of the chip. To describe device scaling, we introduce a constant *scaling factor* $S > 1$. All horizontal and vertical dimensions of the *large-size* transistor are then divided by this scaling factor to obtain the scaled device.


GATE
S
D
W' = W / S
OXIDE
$t_{ox}' = t_{ox} / S$
$X_j' = X_j / S$
$N_D' = N_D * S$
$N_D' = N_D * S$
L' = L / S
SUBSTRATE DOPING $N_A' = N_A * S$

Scenario #1: Constant-Field Scaling

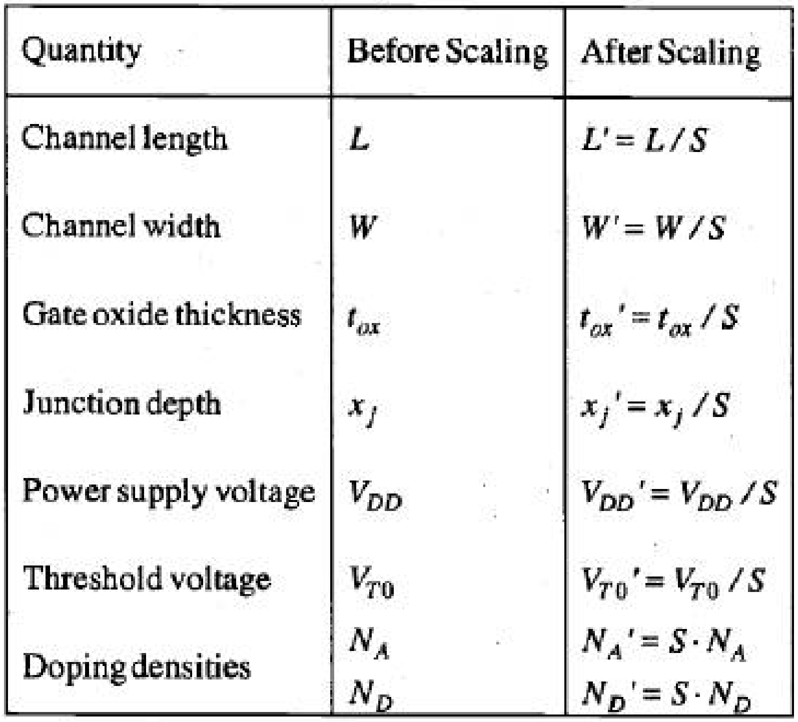
- Voltages and MOSFET dimensions are scaled by the same factor S >1, so that the **electric field remains unchanged**



1. Constant field scaling or full scaling :

- ➢ Magnitude of internal electric fields is kept constant.
- ➢ Only lateral dimensions are changed.
- ➢ Threshold voltage is also effected.

Consequences of Constant Field Scaling :



Quantity	Before Scaling	After Scaling
Channel length	L	$L' = L / S$
Channel width	W	$W' = W / S$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox} / S$
Junction depth	x_j	$x_j' = x_j / S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD} / S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{T0} / S$
Doping densities	N_A N_D	$N_A' = S \cdot N_A$ $N_D' = S \cdot N_D$

$$C_{ox}' = \frac{\varepsilon_{ox}}{t_{ox}'} = S \cdot \frac{\varepsilon_{ox}}{t_{ox}} = S \cdot C_{ox}$$

$$\begin{aligned} I_D'(lin) &= \frac{k_n'}{2} \cdot \left[2 \cdot \left(V_{GS}' - V_T' \right) \cdot V_{DS}' - V_{DS}'^2 \right] \\ &= \frac{S \cdot k_n}{2} \cdot \frac{1}{S^2} \cdot \left[2 \cdot \left(V_{GS} - V_T \right) \cdot V_{DS} - V_{DS}^2 \right] = \frac{I_D(lin)}{S} \end{aligned}$$

$$I_D'(sat) = \frac{k_n'}{2} \cdot \left(V_{GS}' - V_T' \right)^2 = \frac{S \cdot k_n}{2} \cdot \frac{1}{S^2} \cdot \left(V_{GS} - V_T \right)^2 = \frac{I_D(sat)}{S}$$

Impact of Constant-Field Scaling

(a) MOSFET gate capacitance:

$$C'_{gate} = L'W'C'_{ox} = \left(\frac{L}{S}\right)\left(\frac{W}{S}\right)\cdot\left(\frac{\varepsilon_{ox}}{t_{ox}/S}\right) = \frac{C_{gate}}{S}$$

(b) MOSFET drive current:

$$I'_{DSAT} \propto C'_{ox}\frac{W'}{L'}\left(V'_{DD}-V'_{T}\right)^2 \cong \left(SC_{ox}\right)\left(\frac{W/S}{L/S}\right)\left(\frac{V_{DD}-V_{T}}{S}\right)^2 \propto \frac{I_{DSAT}}{S}$$

(c) *Intrinsic gate delay* :

$$\frac{C'_{gate}V'_{DD}}{I'_{DSAT}} = \frac{\left(C_{gate}/S\right)\left(V_{DD}/S\right)}{\left(I_{DSAT}/S\right)} = \left(\frac{C_{gate}V_{DD}}{I_{DSAT}}\right)\bullet\frac{1}{S}$$

Impact of Constant-Field Scaling (cont'd)

(d) Device density:

area required per transistor $\propto W'L'$

# of transistors per unit area $\propto \dfrac{1}{W'L'} = \dfrac{1}{(W/S)(L/S)} = \dfrac{S^2}{WL}$

(e) Power dissipated per device:

$$P'_{peak} = I'_{DSAT} \cdot V'_{DD} = \left(\frac{I_{DSAT}}{S}\right) \cdot \left(\frac{V_{DD}}{S}\right) = \frac{P_{peak}}{S^2}$$

(f) Power density:

$$P'_{peak} \cdot \frac{1}{W'L'} = \frac{P_{peak}}{S^2} \cdot \left(\frac{1}{(W/S)(L/S)}\right) = \frac{P_{peak}}{WL}$$

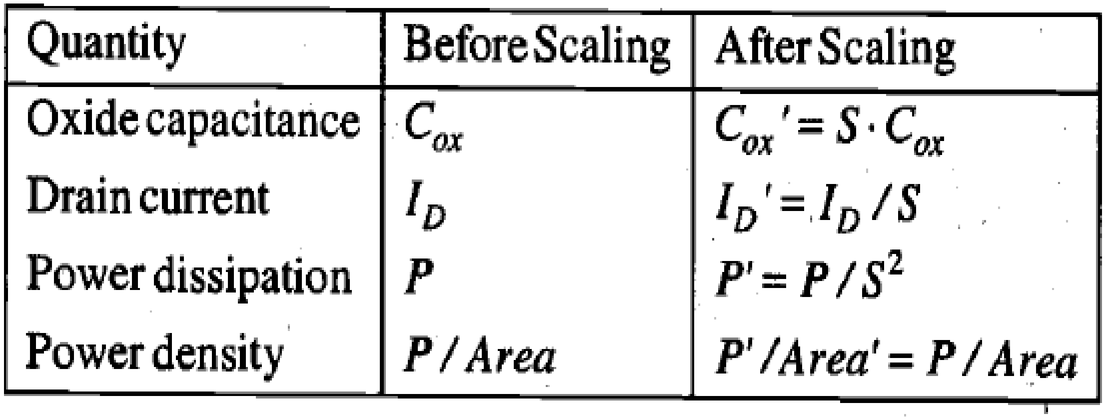
✓ **Power consumed per function is reduced by S^2**

Note that with the device area reduction by S^2 discussed earlier, we find the *power density* per unit area remaining virtually unchanged for the scaled device.

Most significant reduction :

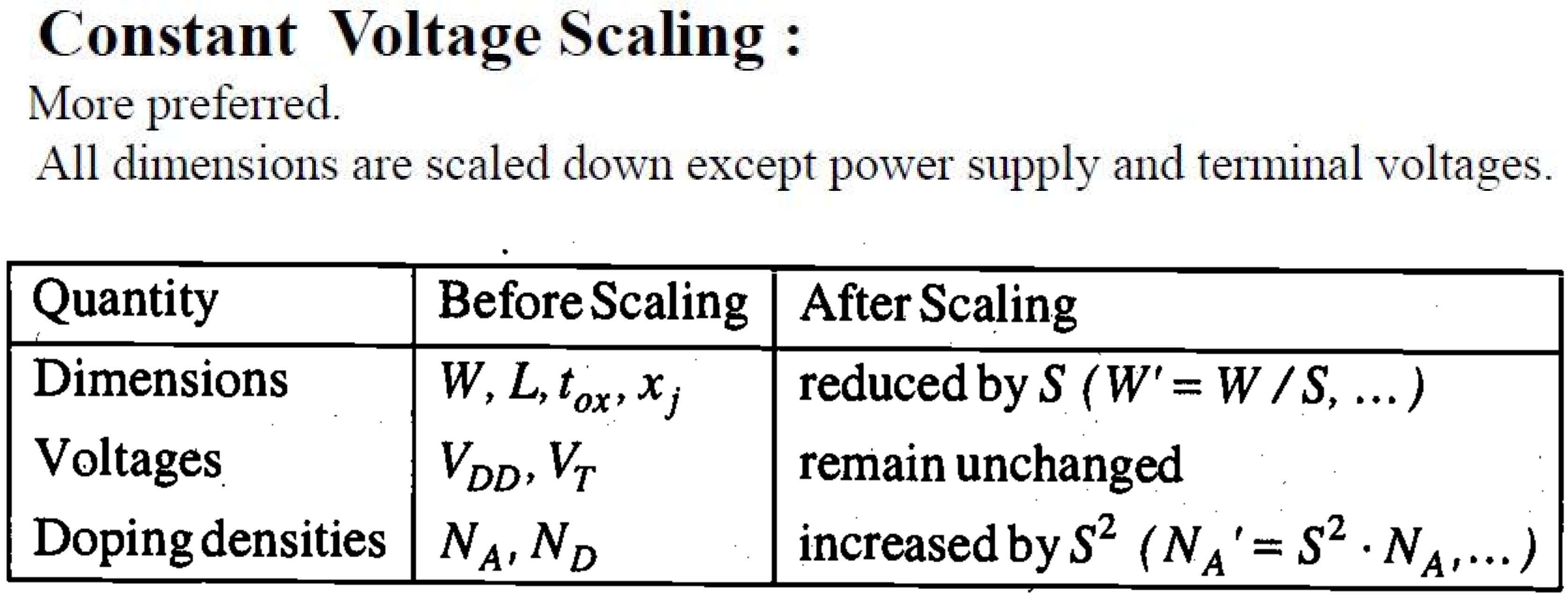
Power dissipation is reduced by a factor of S^2 as $P' = P/S^2$

- Power density remains unchanged.
- Gate capacitance is scaled down as $C_g' = C_g/S$
- Overall performance improvement.



Quantity	Before Scaling	After Scaling
Oxide capacitance	C_{ox}	$C_{ox}' = S \cdot C_{ox}$
Drain current	I_D	$I_D' = I_D / S$
Power dissipation	P	$P' = P / S^2$
Power density	$P / Area$	$P' / Area' = P / Area$

Finally, the Poisson equation describing the relationship between charge densities and electric fields dictates that the charge densities must be *increased* by a factor of S in order to maintain the field conditions.



Constant Voltage Scaling :

More preferred.

All dimensions are scaled down except power supply and terminal voltages.

Quantity	Before Scaling	After Scaling
Dimensions	W, L, t_{ox}, x_j	reduced by S $(W' = W / S, \ldots)$
Voltages	V_{DD}, V_T	remain unchanged
Doping densities	N_A, N_D	increased by S^2 $(N_A' = S^2 \cdot N_A, \ldots)$

- In constant-voltage scaling, all dimensions of the MOSFET are reduced by a factor of *S,* as in full scaling. The power supply voltage and the terminal voltages, on the other hand, remain unchanged.
- The doping densities must be increased by a factor of s^2 in order to preserve the charge-field relations.

$$I_D'(lin) = \frac{k_n'}{2} \cdot \left[2 \cdot (V_{GS}' - V_T') \cdot V_{DS}' - V_{DS}'^2\right]$$

$$= \frac{S \cdot k_n}{2} \cdot \left[2 \cdot (V_{GS} - V_T) \cdot V_{DS} - V_{DS}^2\right] = S \cdot I_D(lin)$$

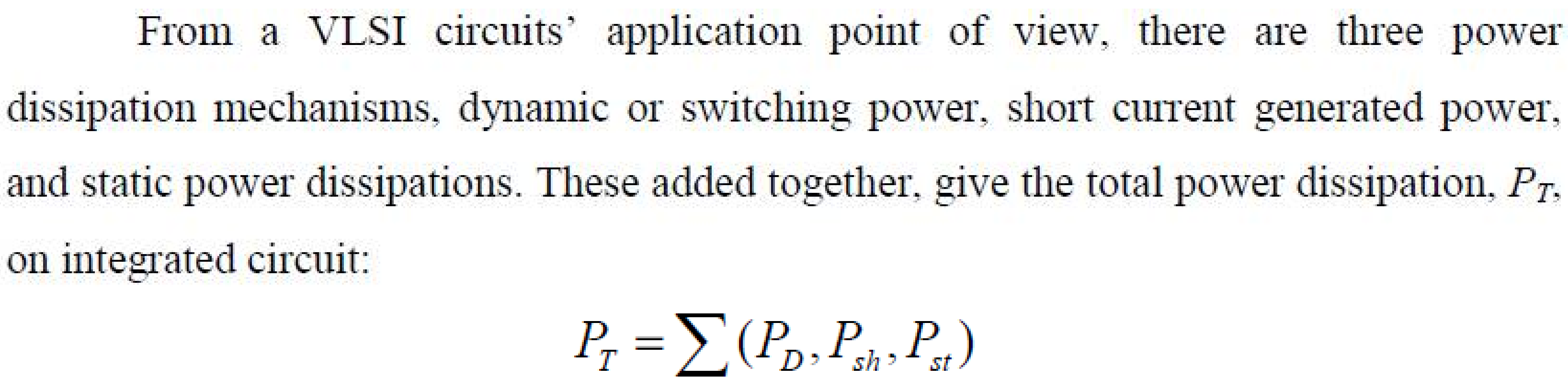
$$I_D'(sat) = \frac{k_n'}{2} \cdot (V_{GS}' - V_T')^2 = \frac{S \cdot k_n}{2} \cdot (V_{GS} - V_T)^2 = S \cdot I_D(sat)$$

$$P' = I_D' \cdot V_{DS}' = (S \cdot I_D) \cdot V_{DS} = S \cdot P$$

Quantity	Before Scaling	After Scaling
Oxide capacitance	C_{ox}	$C_{ox}' = S \cdot C_{ox}$
Drain current	I_D	$I_D' = S \cdot I_D$
Power dissipation	P	$P' = S \cdot P$
Power density	$P / Area$	$P'/Area' = S^3 \cdot (P / Area)$

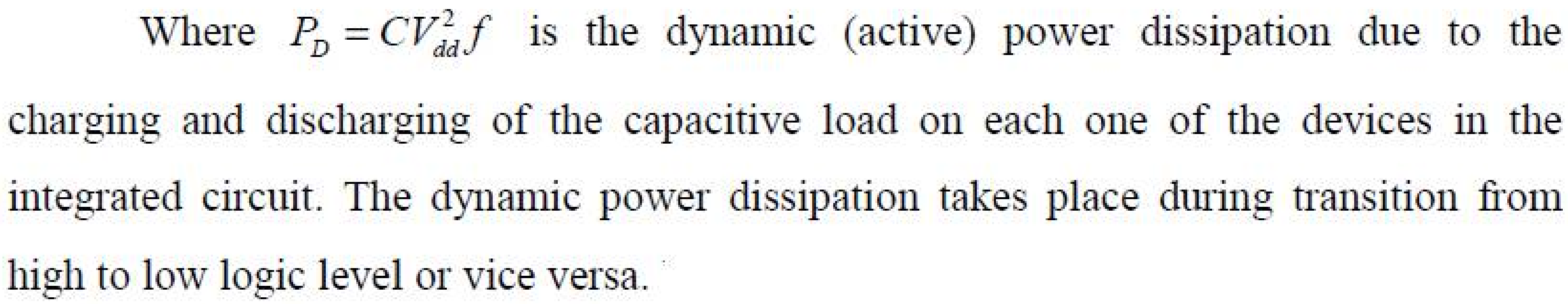
- To summarize, constant-voltage scaling may be preferred over full (constant-field) scaling in many practical cases because of the external voltage-level constraints.
- However, that constant-voltage scaling increases the drain current density and the power density by a factor of S^3.
- This large increase in current and power densities may eventually cause serious reliability problems for the scaled transistor, such as electromigration, hot-carrier degradation, oxide breakdown, and electrical over-stress.

Power Dissipation



From a VLSI circuits' application point of view, there are three power dissipation mechanisms, dynamic or switching power, short current generated power, and static power dissipations. These added together, give the total power dissipation, P_T, on integrated circuit:

$$P_T = \sum (P_D, P_{sh}, P_{st})$$

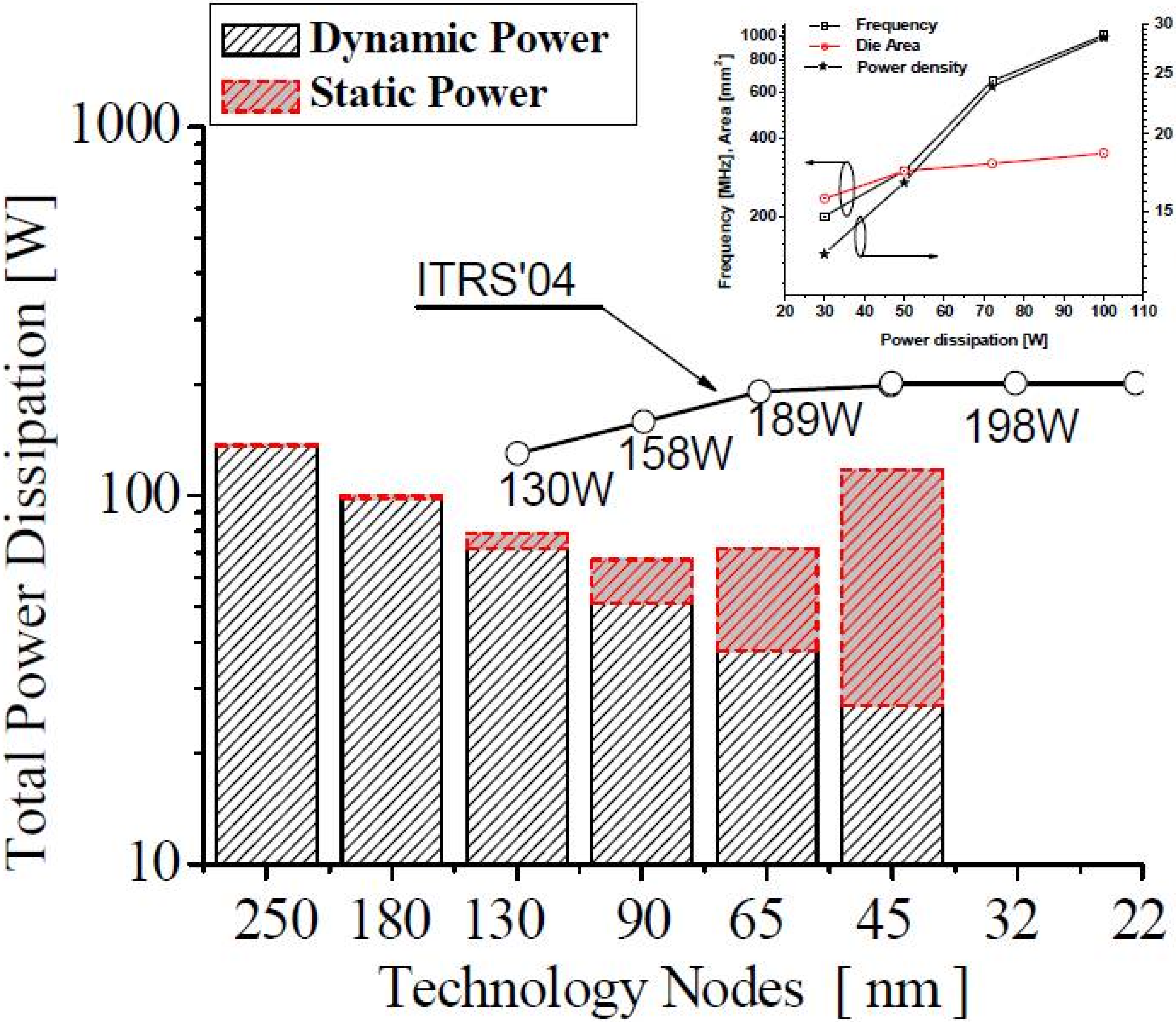


Where $P_D = CV_{dd}^2 f$ is the dynamic (active) power dissipation due to the charging and discharging of the capacitive load on each one of the devices in the integrated circuit. The dynamic power dissipation takes place during transition from high to low logic level or vice versa.

The second term in equation $P_{sh} = V_{dd} I_{short}$ is the power dissipation due to occurrence of short circuit currents. This depends generally on the architecture of the circuit. Usually this is not the main component of power dissipation.

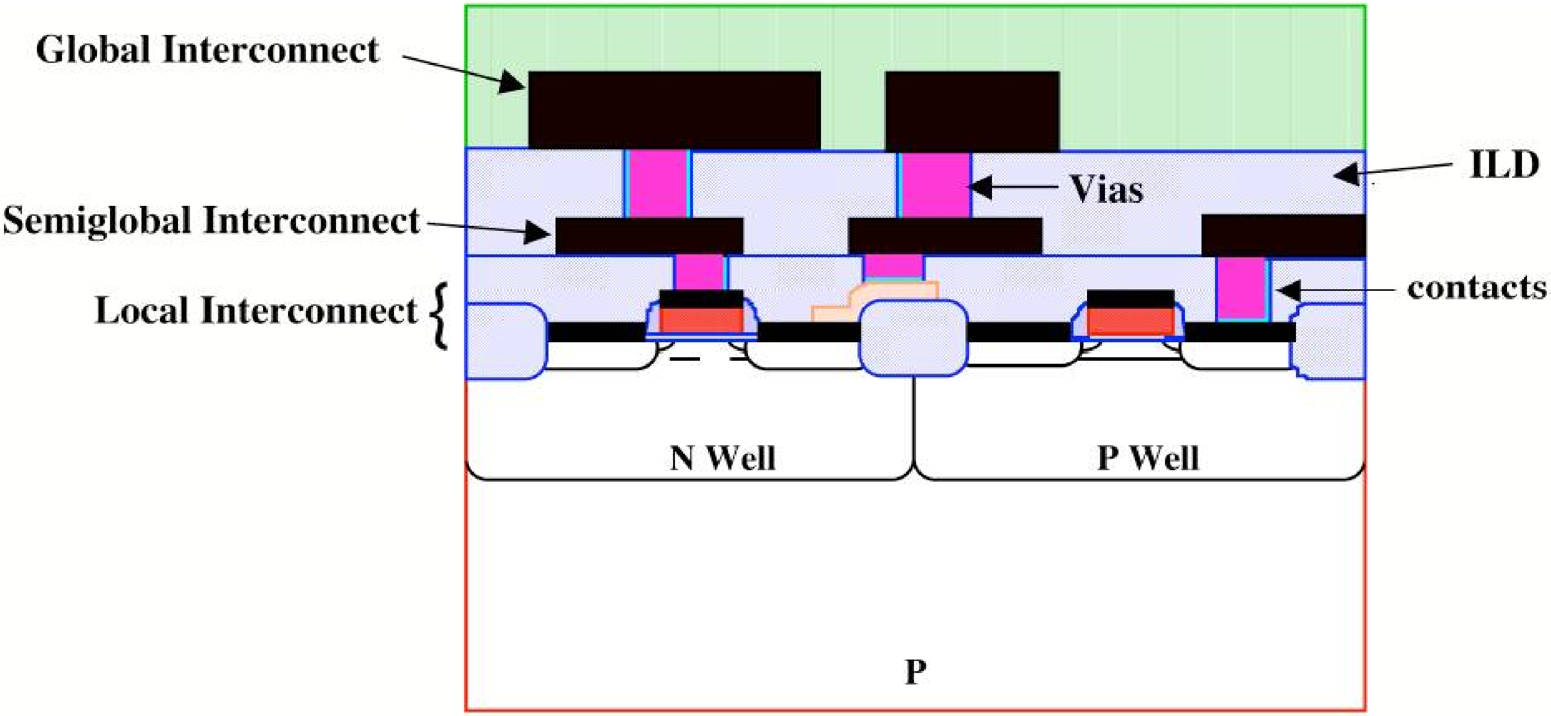
The third component of the total power dissipation is the static power dissipation, $P_{st} = V_{dd} I_{leak}$, which occurs as a result of the cumulative leakage current contributed from all devices in the circuit.

By far the highest power consumption in present circuits comes from the dynamic activity of the devices in the circuit. The dynamic power dissipation is directly proportional to the square of the supply voltage. Although the power supply voltage is reducing as a result of device scaling, due to this quadratic relationship between P_D and V_{dd}, dynamic activity, still accounts for substantial power dissipation.


Dynamic Power
Static Power
Total Power Dissipation [W]
1000
100
10
ITRS'04
130W
158W
189W
198W
250
180
130
90
65
45
32
22
Technology Nodes [nm]
Frequency
Die Area
Power density
Frequency [MHz], Area [mm^2]
1000
800
600
400
200
Power dencity [W/cm^2]
30
25
20
15
20
30
40
50
60
70
80
90
100
110
Power dissipation [W]

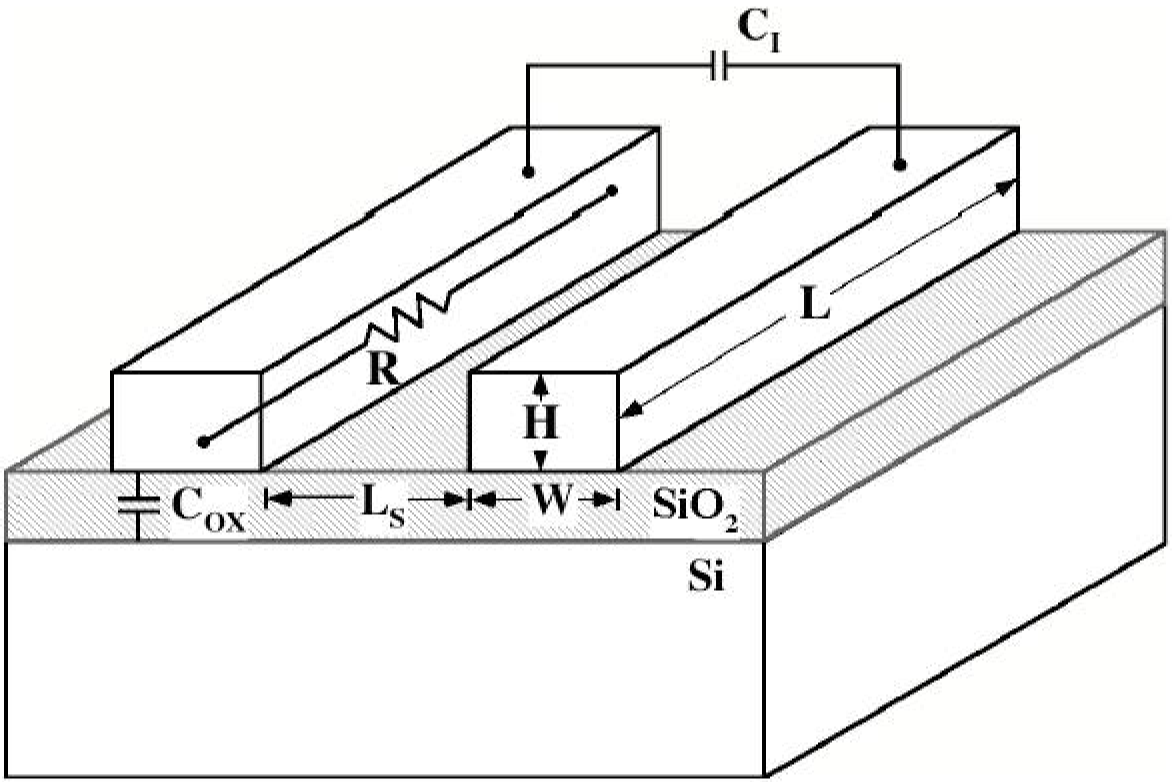
Scaling of Interconnections

Once the active devices and regions are fabricated they must be electrically connected to each other to make circuits. They must also be connected to the outside world through their inputs and outputs on bonding pads. Making these connections is the job of contacts, vias and interconnects. Separating the interconnects from each other is the job of dielectric layers. All of these components are part of the "metallization" or "backend" structure.



- Interconnects can either be global or local. In general, local interconnects are the first, or lowest, level of interconnects. They usually connect gates, sources and drains in MOS technology, and emitters, bases, and collectors in bipolar technology.
- In MOS technology a local interconnect, polycrystalline silicon, also serves as the gate electrode material.
- Global interconnects, mostly made of Al, are generally all of the interconnect levels above the local interconnect level. They often travel over large distances, between different devices and different parts of the circuit, and therefore are always low resistant metals.

Separating interconnects from each other and from the active areas and devices are dielectric materials. Those dielectric layers separating one global interconnect level from another are called intermetal dielectrics, or IMD. (Some call these interlevel dielectrics, or ILD.) Vias connect interconnects through these layers. The layer separating global interconnects from both the substrate and local interconnects, through which the contacts are made, are given a variety of names: first level dielectric, dielectric-1, poly-gate dielectric, pre-metal dielectric, etc. - anything but intermetal dielectric.



$$R = \rho \frac{L}{WH}$$

$$C_{ox} = K_{ox}\varepsilon_o \frac{WL}{X_{ox}}$$

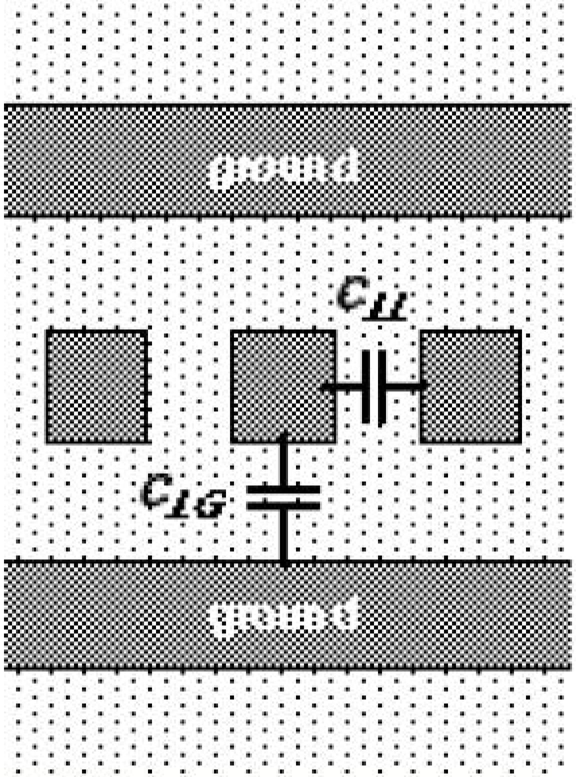
$$C_I = K_{ox}\varepsilon_o \frac{HL}{L_S}$$

where ρ is the interconnect's resistivity, and L, W, and H are the interconnect's length, width and height, respectively.

X_{ox} and K_{ox} are the oxide thickness and dielectric constant, respectively, and ε_o is the permittivity of free space.

So think about reduction of parameters for local and global interconnects

Crosstalk due to capacitive coupling



Higher Packing Density

⇓

Decreased Space
Between Interconnects

⇓

Higher crosstalk